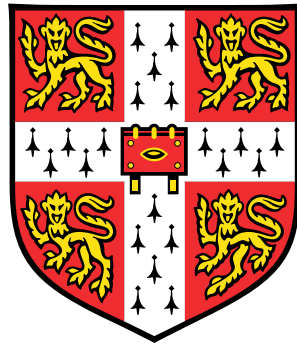


High power wide bandgap cascode switching circuits



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This dissertation is submitted for the degree of
Doctor of Philosophy

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text. This dissertation contains 59,298 words including appendices, bibliography, footnotes, tables and equations and has 93 figures.

Philip Garsed

June 2015

Publications

The following publications have been produced during the course of this research:

- Singh, S.K.; Guédon, F.; Garsed, P.J.; McMahon, R.A., "Half-bridge SiC inverter for hybrid electric vehicles: Design, development and testing at higher operating temperature," Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on , vol., no., pp.1,6, 27-29 March 2012
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Abstract

Emerging wide bandgap (WBG) power transistors are capable of improving the efficiency of mains voltage power electronic circuits. Several commercial WBG transistors are now available, but all exhibit undesirable gate drive characteristics. The cascode circuit has been suggested as a solution to this problem: WBG cascodes improve the switching speed, gate characteristics and noise immunity of devices, at the expense of greater on-state resistance.

WBG cascodes have not, however, been widely accepted in commercial applications. Previous research has typically been too application-specific, with little practical information available for design engineers wishing to use them.

This thesis addresses these shortcomings through a comprehensive investigation of practical design considerations for switch-mode cascode circuits. A SPICE simulation and simplified mathematical model are developed as design tools to give a detailed insight into cascode hard-switching behaviour and to aid cascode optimisation and device selection.

The effects of the cascode configuration on static (DC) device performance are quantified for a silicon super-junction (SJ) metal-oxide-semiconductor field-effect transistor (MOSFET), silicon carbide (SiC) junction field-effect transistor JFET and SiC MOSFET. The on-state resistance penalty of the cascode configuration is shown to be modest and potentially mitigated by careful selection of HV transistor gate bias.

There are few advantages to using silicon SJ MOSFETs in a cascode configuration, but both SiC MOSFET and JFET cascodes benefit from improved gate drive, reverse conduction and switching characteristics. SiC MOSFETs are shown to be better suited to efficient high temperature operation, while SiC JFETs are more appropriate for high current applications.

Cascode switching losses are shown to be reduced compared to standalone devices, although reverse recovery losses can counteract this. Methods of controlling switching transients using gate resistors or feedback capacitors are investigated and shown to be effective.

The effects of stray inductance on cascode switching are quantified experimentally for the first time. This corroborates other work and informs the layout of cascode circuits. The resilience of cascodes to severe $\frac{dV}{dt}$ is also demonstrated.

The findings of this thesis are summarised in a practical design guide aimed at design engineers who wish to use this useful circuit.

Contents

Contents	i
List of Figures	v
List of Tables	ix
1 Introduction	17
1.1 Energy efficiency as a global priority	17
1.2 Electrical systems as a driver of efficiency	19
1.3 Developments in power electronics	21
1.4 Aims of the work	23
1.5 Summary of the thesis	24
1.6 Contributions	25
2 Background	27
2.1 Introduction	27
2.2 Modern silicon power devices	27
2.3 Wide bandgap semiconductors	29
2.4 Silicon Carbide	31
2.5 Gallium Nitride	37
2.6 WBG device selection	40
2.7 The cascode circuit	40
2.8 The wide bandgap cascode	44
2.9 Conclusion	51
3 Experimental techniques	53
3.1 Introduction	53
3.2 Test PCB	53
3.3 Clamped inductive load	60

3.4	Test set-up	62
3.5	Curve tracing	62
3.6	Oscilloscope and probe selection	65
3.7	Rogowski probe $\frac{dV}{dt}$ dependence	70
3.8	PCB inductance characterisation	74
3.9	Summary	82
4	Modelling a wide bandgap cascode switch	85
4.1	Introduction	85
4.2	SPICE simulation	85
4.3	Modelling approach	86
4.4	SiC JFET Modelling	87
4.5	Modelling a SiC JFET cascode	107
4.6	Validating the SPICE model	109
4.7	Simplifying the switching model	113
4.8	Modelling assumptions	115
4.9	Simplifying the switching model	117
4.10	Validating the idealised switching model	127
4.11	Implications of the simplified model	131
4.12	Cascode modelling conclusions	134
5	Static characterisation	135
5.1	Introduction	135
5.2	Device selection	135
5.3	I-V Characteristics	137
5.4	Cascode reverse conduction as a free-wheel path	149
5.5	High temperature operation	156
5.6	Static characteristics: conclusions	163
6	Dynamic characteristics	165
6.1	Introduction	165
6.2	Cascode switching performance	165
6.3	Comparative switching performance	167
6.4	Gate resistance control of cascode circuits	178
6.5	Effect of stray inductance on cascode circuits	187
6.6	Control of $\frac{dV}{dt}$ transients	192
6.7	Cascode immunity to $\frac{dV}{dt}$ transients	198

6.8	Reverse recovery behaviour	203
6.9	Conclusion	206
7	Conclusions	209
7.1	Summary	209
7.2	General conclusions	209
7.3	Cascode design guide	210
7.4	Further work	216
	References	219
A	Semisouth SiC JFET SPICE model	237
B	SiC JFET hybrid model	239
C	PCB design drawings	241
C.1	Schematics	241
C.2	Layout	241
D	Clamped inductive load driver code	247
E	Effects of HV gate and drain inductance	249

List of Figures

1	Schematic of cascode circuit used for simplified model	xi
1.1	Mean monthly atmospheric carbon dioxide concentrations 1980 - 2015	18
1.2	A contemporary EU energy label	18
1.3	Percentage electricity generation in EU by source in 2012	20
1.4	Victorian tramcar, utilising crude and lossy power control	21
1.5	A simple cascode circuit	23
2.1	Manufactured devices and limits of on-state resistance with blocking voltage for silicon, SiC and GaN	31
2.2	Power handling and switching frequency capability of various semiconductor devices	32
2.3	Synthetic Moissanite as a diamond substitute in the author's wife's engage- ment ring	32
2.4	Typical structure of a SiC MOSFET	34
2.5	Structure of SiC vertical JFET	35
2.6	Gate drive methods proposed by Domes and Round for SiC JFETs	37
2.7	Basic structure of a typical GaN HEMT	39
2.8	A power cascode circuit	41
2.9	Original drawings for MOSFET-controlled power cascodes from Baliga's 1987 patent	43
2.10	The 'stack cascode' concept	45
2.11	The capacitor-clamped cascode concept	48
2.12	The 'cascode light' configuration	49
3.1	A bare test PCB	54
3.2	Grounding methods for different passive voltage probes	55
3.3	Copper measurement loop and Rogowski coil	57
3.4	Wire bonds at JFET die gate	59

3.5	Diagram of clamped inductive test circuit	61
3.6	Test set-up for clamped inductive load	62
3.7	Measurement of Si SJ cascode I-V characteristic	63
3.8	Arrangement of short pulse-width curve tracing set-up	64
3.9	Resistive load voltage derived from voltage measurements and Rogowski current measurements de-skewed by +17.0 ns	69
3.10	Relationship between $\frac{dV_{DS(casc)}}{dt}$ and Rogowski coil I_D measurement error during cascode voltage rise and fall	72
3.11	Switching waveforms comparing I_D measured with Rogowski coil with corrected I_D measurements, actual I_D measurement and $V_{DS(casc)}$	73
3.12	Inductance measurements for three PCB power tracks	78
3.13	Connection of pigtailed to measure PCB track inductance	79
3.14	PCB inductance measurement sections	80
3.15	Coilcraft mini-spring coil inductors	81
3.16	Measured vs. nominal additional inductance for 20 inductance measurements	82
4.1	Comparison between simulated and measured JFET I-V characteristics	89
4.2	I-V curve for Semisouth SJDP120R085 SiC JFET using short pulse-width measurement technique vs. Tektronix 371A curve tracer measurements	90
4.3	I-V curve for Semisouth SJDP120R085 SiC JFET using short pulse-width measurement technique vs. Semisouth SPICE model simulations	91
4.4	Effect of electric field on carrier velocity	92
4.5	$\sqrt{I_D}$ vs V_{GS} relationship for SJDP120R05 SiC JFET	97
4.6	Geometric SPICE MOSFET parameters and their interpretation for a SiC vertical JFET	98
4.7	I-V curve from experimental measurements vs. MOS3-based SPICE simulations for Semisouth SJDP120R085 SiC JFET	100
4.8	I-V curve from MOS3-based SPICE model of Semisouth SJDP120R085 SiC JFET, for V_{DS} of 1 - 1000 V	101
4.9	Parasitic capacitance vs V_{DS} from datasheet curves vs. VDMOS capacitance model SPICE simulations for Semisouth SJDP120R085 SiC JFET	103
4.10	Comparison of experimentally measured gate-source/gate-drain diode characteristics with idealised SPICE model	104
4.11	Hybrid SPICE model of SJDP120R085 JFET as implemented in LTSPICE	106
4.12	I-V curves from datasheet figures compared to SPICE simulation results for LV transistors	107

4.13	Parasitic capacitance vs V_{DS} from datasheet figures compared to SPICE simulation results for LV transistors	108
4.14	SPICE representation of SOT-23 LM5114 gate driver	108
4.15	Complete SPICE SiC JFET cascode clamped inductive load model	110
4.16	Turn-on and turn-off behaviour of a SiC JFET cascode vs. SPICE model	111
4.17	Schematic of cascode circuit used for simplified model	115
4.18	Turn-on and turn-off behaviour of a SiC JFET cascode vs. idealised model	118
4.19	Equivalent circuit for stage I	119
4.20	Equivalent circuit for stage II	119
4.21	Equivalent circuit for stage III	120
4.22	Equivalent circuit for stage IV	121
4.23	Equivalent circuit for stage V	122
4.24	Equivalent circuit for stage VI	122
4.25	Equivalent circuit for stage VII	123
4.26	Equivalent circuit for stage VIII	124
4.27	Equivalent circuit for stage IX	125
4.28	Equivalent circuit for stage X	126
5.1	I-V curves for individual devices in forward and reverse conduction	141
5.2	Simulated divergence between SJDP120R085/FDMS5352 cascode and FDMS5352 I-V curves	143
5.3	I-V curves for cascode devices in forward and reverse conduction	145
5.4	Gate control characteristics at $V_{DS} = 10$ V for all devices combinations	147
5.5	$R_{DS(ON)}$ for all device combinations at $V_{DS} = 0$ V	148
5.6	Reverse conduction characteristics for individual and cascoded high voltage devices	155
5.7	$R_{DS(ON)}$ for SiC MOSFET and SiC JFET from 25 - 200 °C	158
5.8	Change in SiC MOSFET transfer characteristic from 25 to 200 °C	159
5.9	Change in V_T at $I_D = 100$ mA for SiC MOSFET and SiC JFET and change in JFET gate-source diode V_f at $I_G = 100$ mA from 25 to 200 °C.	160
5.10	Temperature dependence of specific $R_{DS(ON)}$ for SiC devices at 1A from 25 to 200 °C	162
6.1	Datasheet C_{DG} characteristic for Infineon IPW65R080CFD Si SJ MOSFET	169
6.2	Switching characteristics for individual HV transistors	171
6.3	Switching characteristics for cascoded HV transistors	174
6.4	Switching times for individual and cascode transistors	176

6.5	Switching losses for individual and cascode transistors	177
6.6	Turn-on waveforms for $R_{G(HV)} = 1.5, 2.2, 3.3, 4.7$ and 6.8Ω	180
6.7	Turn-off waveforms for $R_{G(HV)} = 1.5, 2.2, 3.3, 4.7$ and 6.8Ω	182
6.8	Turn-on waveforms for $R_{GH(LV)} = 1, 2.2, 4.7, 10, 22, 47$ and 100Ω	183
6.9	Turn-off waveforms for $R_{GL(LV)} = 10, 22, 47, 100, 220$ and 470Ω	185
6.10	Contour plot showing trade-off between $V_{DS(LV)}$ in Volts vs. turn-off energy loss in μJ for various values of $R_{GL(LV)}$ and $R_{G(HV)}$	187
6.11	Turn-on waveforms for $L_{(S,add)} = 0, 2.5, 5, 8, 12.5$ and 18.5 nH	189
6.12	Turn-off waveforms for $L_{(S,add)} = 0, 2.5, 5, 8, 12.5$ and 18.5 nH	190
6.13	$\frac{dV}{dt}$ control methods originally proposed by Aggeler et al.	193
6.14	Effect of adding 0, 16.5, 33, 66 and 100 pF between SiC MOSFET drain and gate in cascode configuration.	195
6.15	Effect of adding 0, 33, 66 and 100 pF between SiC MOSFET drain and gate in cascode configuration.	196
6.16	Comparison of simulated $\frac{dV}{dt}$ effects for individual JFET, cascoded JFET and TVS protected JFET cascode in single phase leg.	199
6.17	Comparison between reverse recovery of SiC MOSFET cascode and SiC Schottky diode when switching 25 A at 600 V	204
C.1	Test PCB schematic drawings	244
C.2	Test PCB layout	246
E.1	Switching waveforms for $L_{(D,add)} = 0, 2.5, 5, 8, 12.5$ and 18.5 nH	249
E.2	Switching waveforms for $L_{(G,add)} = 0, 2.5, 5, 8$ and 12.5 nH	250

List of Tables

1	Summary of notation	xiii
1.1	EU electricity consumption and potential energy saving through the use of power electronics	20
2.1	Properties and normalised unipolar figures of merit for silicon, SiC and GaN semiconductors	30
3.1	Estimated bounds for bond wire inductance.	60
3.2	Properties of oscilloscope probes used in this work	67
3.3	Skew calibration of oscilloscope probes	69
3.4	Details of PCB inductance measurement sections	80
3.5	Measured PCB inductances for upper and lower switches (nH). Measurements on the same line are for tracks with similar PCB layout.	81
4.1	List of SPICE parameters for MOS3 model for modelling vertical JFET	100
4.2	List of SPICE parameters for VDMOS model for modelling vertical JFET capacitances	102
4.3	List of SPICE parameters for idealised diode model for modelling vertical JFET gate diodes	105
4.4	Comparison between datasheet threshold voltage and voltage at which peak g_m reached	116
4.5	Summary of equations derived for simplified cascode switching model	128
4.6	List of model parameter values used in simplified model of figure 4.18	129
4.7	Equations to describe key performance parameters	132
5.1	Properties of transistors used	137
6.1	Gate resistances used for control of standard and cascode switches	168
6.2	Device parameters relevant to switching	168

Notation

The large number of voltages, currents, resistances, capacitance and inductances relevant to the operation of the cascode circuit require unique symbols to make concise description of circuit operation possible. Table 1 summarises the notation used to describe circuits in the following experimental chapters.

The relevance of this notation to the cascode circuit is shown in figure 1.

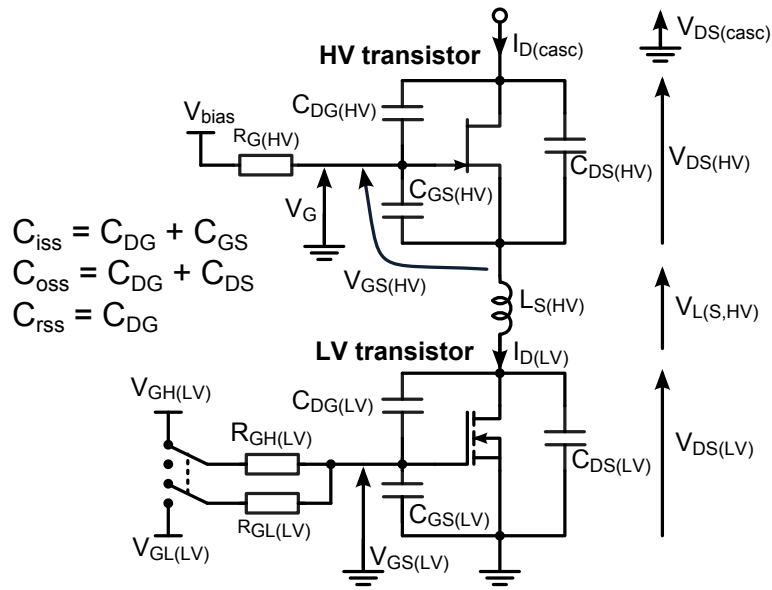


Figure 1: Schematic of cascode circuit used for simplified model

Abbreviation	Description	Comments
HV	High voltage	Also shorthand denoting specific device in cascode circuits
LV	Low voltage	
casc	Cascode	Refers to parameters treating cascode circuit as a single device.
int	Internal	A parameter internal to a transistor
RESISTANCES		
R_G	Gate resistor	Single gate resistor controlling both turn-on and turn-off
R_{GH}	Turn-on gate resistor	Resistor responsible only for turn-on charging of gate
R_{GL}	Turn-off gate resistor	Resistor responsible only for turn-off charging of gate
$R_{DS(ON)}$	On-state channel resistance	Usually for fully-enhanced channel
R_{damp}	Damping resistance	Damps parasitic oscillations. Determined experimentally
CAPACITANCES		
C_{iss}	Device input capacitance	$= C_{GS} + C_{DG}$
C_{oss}	Device output capacitance	$= C_{DG} + C_{DS}$
C_{DG}	Device drain-gate capacitance	$= C_{rss}$, Voltage dependent
C_{GS}	Device gate-source capacitance	Voltage dependent
C_{DS}	Device drain-source capacitance	Voltage dependent
C_A	$\frac{dV}{dt}$ limiting capacitance (see section 6.6)	Additional capacitance between HV drain and HV gate
C_B	$\frac{dV}{dt}$ limiting capacitance (see section 6.6)	Additional capacitance between HV drain and LV gate
INDUCTANCES		
L_S	Inductance at transistor source	V_{GS} assumed to include effect of this inductance
L_{power}	Inductance of clamped inductive load	Typically large (approximates current source)

Abbreviation	Description	Comments
VOLTAGES		
V_{GH}	Gate driver turn-on voltage	Gate driver output voltage at turn-on
V_{GL}	Gate driver turn-off voltage	Gate driver output voltage at turn-off (typically 0 V)
V_{GS}	Device gate-source voltage	Relevant to control and device ratings
V_{DS}	Device drain-source voltage	Relevant to device ratings
V_{GD}	Device gate-drain voltage	Relevant to device ratings during reverse conduction
V_T	Transistor threshold voltage	Gate-source voltage at which transistor begins to turn on
V_{bias}	Gate bias voltages	HV transistor in cascode configuration only
V_{DC}	DC bus voltage	Rated voltage in clamped inductive load
V_f	Diode forward voltage	Additional subscript may relate to specific diode
$\frac{dV}{dt}$	Rate of change of voltage	Specific voltage denoted by subscript
CURRENTS		
I_D	Device current at drain	Typically $I_D = I_S + I_{Miller}$
I_S	Device current at source	
I_L	Current in clamped inductive load inductor	Largely constant for large I_L
I_{miller}	Miller current	Flows through C_{DG} and gate resistance when V_{DS} changes
$\frac{dI}{dt}$	Rate of change of current	Specific current denoted by subscript
OTHER PARAMETERS		
g_m	Device forward transconductance	Rate of change of I_D with changing V_{GS} greater than V_T
τ	Time constant	Denotes time delay

Table 1: Summary of notation. Note that the subscripts HV and LV are used to denote a parameter applying to a particular transistor in the cascode arrangement. The subscript $casc$ denotes a parameter describing the overall behaviour of a cascode circuit, the subscript int indicates a value internal to a device and $\hat{}$ denotes a peak value

Nomenclature

Roman Symbols

AC	Alternating current
AlN	Aluminium nitride
BJT	Bipolar junction transistor
C	Diamond
CrM	Critical conduction mode
DC	Direct current
EMI	Electromagnetic interference
EPC	Efficient Power Conversion Corporation
ESBT	Emitter switched bipolar transistor
ESR	Equivalent series resistance
EU	European Union
FET	Field-effect transistor
GaN	Gallium nitride
GTO	Gate turn-off
HEMT	High-electron-mobility transistor
HV	High voltage (above 100 V in this context)
IC	Integrated circuit

IF	Intermediate frequency
IGBT	Insulated gate bipolar transistor
JFET	Junction field-effect transistor
LCR	Inductance-capacitance-resistance
LED	Light-emitting diode
LV	Low voltage (below 100 V in this context)
MOSFET	Metal-oxide-semiconductor field-effect transistor
PCB	Printed circuit board
PEM	Power Electronic Measurements Ltd.
PQFN	Power quad flat no-lead
PWM	Pulse-width modulation
RF	Radio frequency
SCR	Silicon controlled rectifier (or thyristor)
SiC	Silicon carbide
SJ	Super-junction
SMA	Subminiature version A
SMD	Surface-mount device
SOLT	Short, open, load, through
SPICE	Simulation program with integrated circuit emphasis
TVS	Transient voltage suppressor
USB	Universal serial bus
VNA	Vector network analyser
WBG	Wide bandgap
ZVS	Zero-voltage switching

Chapter 1

Introduction

1.1 Energy efficiency as a global priority

We live in a world where the production and use of energy is under increasing scrutiny. For years, scientists have warned about the severe potential worldwide impact of anthropogenic global warming [2] and the need to reduce global carbon emissions. These warnings were underlined in March 2015, when for the first time, monthly mean global carbon dioxide concentrations exceeded 400 ppm (figure 1.1). There are also political and economic reasons for concern. World energy markets can be volatile and key suppliers are often in politically unstable regions. Many countries perceive this to be a threat to national security and competitive advantage, causing them to seek greater energy self-sufficiency by investing heavily in domestic energy production.

The efficient use of energy has therefore become an international priority. Most countries have now committed to limiting global temperature increases to below 2 °C by implementing deep cuts in greenhouse gas emissions [3]. Whilst a long-term switch to low-carbon energy sources is an important part of meeting emissions targets, energy efficiency improvements for all energy sources are thought to represent around 40% of the potential for reducing global CO₂ emissions [4]. Meanwhile, for those countries concerned about energy security and competitiveness, energy efficiency is an important way of maximising the returns on their investments.

Where the challenge of the 20th century was providing sufficient energy to meet growing demand, the challenge of the 21st century will be to make better use of our available energy resources.

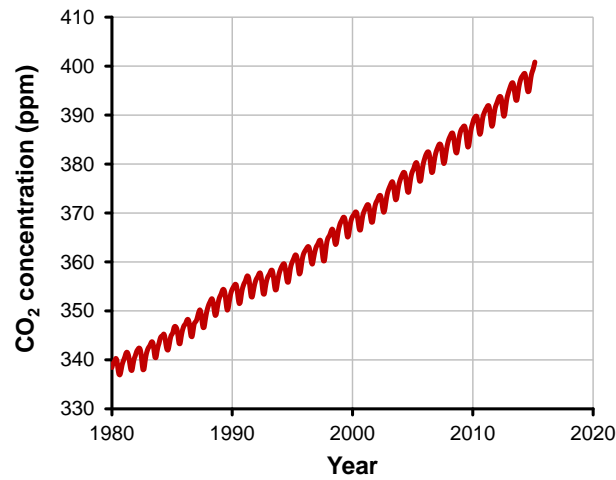


Figure 1.1: Mean monthly atmospheric carbon dioxide concentrations 1980 - 2015 [1]. Note false origin.



Figure 1.2: A contemporary EU energy label [7]

1.1.1 Legislation and market forces

Many governments have attempted to improve overall energy efficiency by introducing legislation. For example, the European Union (EU) has mandated its member states to achieve a 20% reduction in energy use through improved energy efficiency by 2020 [5]. Other schemes such as the European Energy Label (figure 1.2) are aimed at consumers to encourage them to consider efficiency when purchasing household appliances. This scheme provides an incentive for manufacturers to improve efficiency and has helped reduce the energy consumption of most household appliances by between 30 - 70% since 1990 [6].

Independently of legislation, many industries are finding that energy efficiency is an important factor in maintaining a healthy profit margin in competitive global markets. More

efficient industrial systems not only reduce energy costs and avoid punitive measures imposed by governments, but can also improve manufacturing flexibility and reliability.

1.2 Electrical systems as a driver of efficiency

Around 35% of global energy use today is in the form of electrical energy and this is forecast to increase to around 70% by 2040 [8]. Maximising the efficiency of electrical systems is therefore mandatory if energy efficiency targets are to be met.

Electrical systems are increasingly also being seen as a way of improving the efficiency of traditionally non-electrical applications. The emergence of hybrid and all-electric vehicle technology is a prime example of this: by using electric drives in vehicles, energy that would otherwise be lost during braking can be recycled, which greatly increases efficiency in stop-start driving conditions. In other industries, greater electrification translates into lower fuel and running costs. This is currently being seen in the continuing electrification of national rail networks [9] and the wider use of electrical systems in aircraft [10].

1.2.1 The role of power electronics

Power electronics is the key technology that will enable improvements in electrical power conversion efficiency. In 2005, it was estimated that around 30% of all electrical power flowed through power electronic systems between its generation and final use; by 2030, it is anticipated that this figure will be around 80% [11]. The efficiency of power electronic converters is therefore globally significant.

The scale of efficiency improvements possible through the wider application of power electronics must not be underestimated. In the EU, the widespread adoption of efficient power electronic systems is thought to be capable of reducing electrical energy demand by around one quarter, as shown in table 1.1.

In fact, the benefits of more efficient power conversion are of a similar magnitude to those of renewable energy sources. As illustrated by figure 1.3 the potential contribution of more efficient power conversion toward reducing European carbon emissions is far larger than the current combined contribution of all renewable electricity sources. Indeed, the combination of increasing renewable generation capacity and improved power conversion efficiency will go a long way towards de-carbonising the European electricity supply.

There are additional incentives for more efficient power electronics: modern power converters give precise control over power inputs and outputs, allowing the power demands of systems to be matched perfectly to the supply. In industry, this can reduce the size, weight,

Application	Current consumption (% of EU consumption)	Potential energy savings (% of current EU consumption)
Motor control	~50%	5-6%
Lighting	21%	>14%
Data centres/servers	2%	1%
Radio base stations	1%	0.3%
Standby consumption	4%	3.6%
TOTAL	~78%	~24.9%

Table 1.1: EU electricity consumption and potential energy saving through the use of power electronics, for various applications [12].

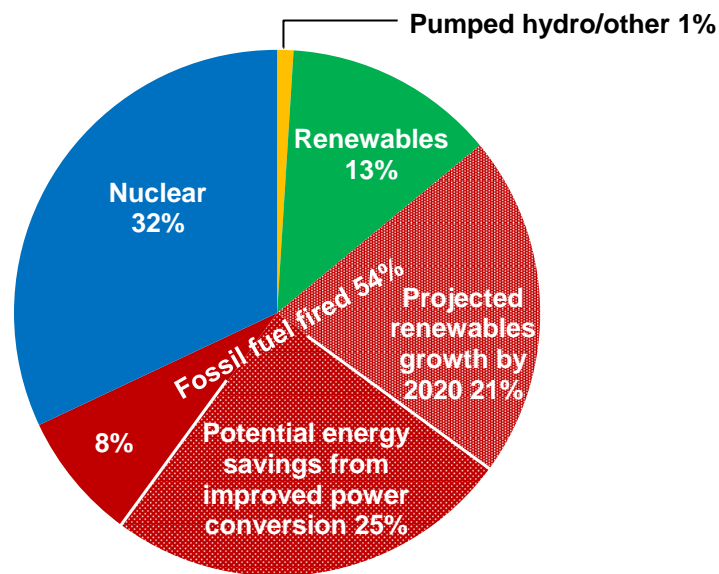


Figure 1.3: Percentage electricity generation in EU by source in 2012. Projected future growth of renewables and potential energy savings from improved power electronics are shown as potential reductions in fossil fuel use [12–14].



Figure 1.4: Victorian tramcar, utilising crude and lossy power control. (Photograph is author's own)

cost and cooling requirements of machinery. In consumer products, the compact and light-weight power converters found in battery chargers and power supplies make portable electronic devices a reality. Power electronics also makes other new efficient technologies possible: the low cost power converters found in compact fluorescent and light-emitting diode (LED) light bulbs are enabling an ongoing revolution in lighting efficacy, which could ultimately further reduce total global electricity consumption by around 6 - 8% [15].

Power electronics will play a globally significant role in increasing energy efficiency, both by improving existing electrical systems and by enabling other efficient technologies. Researching and developing the next generation of power electronic systems is therefore an imperative to fully exploit the potential of these systems.

1.3 Developments in power electronics

1.3.1 Origins

Before the development of power electronics, power conversion was an inefficient business, dependent on simple electro-mechanical rotary converters [16]. The control of electrical power to loads was cruder still: even in high power applications such as electric tramcars, speed control was only possible by changing the series and parallel configuration of traction motors, whilst dissipating excess power in resistor banks [17] (figure 1.4).

This all changed with the invention of the mercury arc rectifier [18] and the thyatron [19] in the early years of the 20th century. For the first time, electrical power could be controlled entirely by electronic circuits without wasting ‘excess’ power and without the need for bulky electrical machines.

1.3.2 Silicon power electronics

Silicon semiconductor power devices were first introduced in 1957 in the form of the silicon controlled rectifier (SCR, or thyristor) [19] and silicon devices have dominated power electronics ever since. Solid-state devices can handle much higher power densities than vacuum tube devices, and are also more efficient and reliable. Subsequent decades have seen the introduction and development of increasingly effective power transistors, from the bipolar junction transistor (BJT) in the 1960s, the power metal-oxide-semiconductor field-effect transistor (MOSFET) in the 1970s, and the insulated gate bipolar transistor (IGBT) in the 1980s [20].

The development of power electronics has been characterised by device improvements driving increases in converter power density and efficiency. Better devices have lower resistive losses when conducting current and waste less energy when being switched on or off. This makes them more efficient, able to operate at higher frequencies and capable of handling higher currents. In a power converter, this means that the size of the passive components, heat-sinking components and the power switches themselves can be reduced, allowing a converter to handle greater electrical power in a given volume. In fact, converter power density power density has approximately doubled every decade since 1970 [21].

1.3.3 Wide bandgap devices

To meet the growing demand for ever more efficient power converters, the performance of power devices must continue to improve. However, as will be shown in the following chapter, modern silicon power devices now operate very close to the fundamental performance limits of silicon. In response, there has been a global effort to research alternative power semiconductors. Today there are two main contenders: silicon carbide (SiC) and gallium nitride (GaN), both of which are types of wide bandgap (WBG) semiconductor. Power transistors made from WBG materials have very attractive properties compared to silicon devices of similar ratings and a number of commercial devices are now available, including SiC junction field-effect transistors (JFETs), SiC MOSFETs and GaN high-electron-mobility transistors (HEMTs).

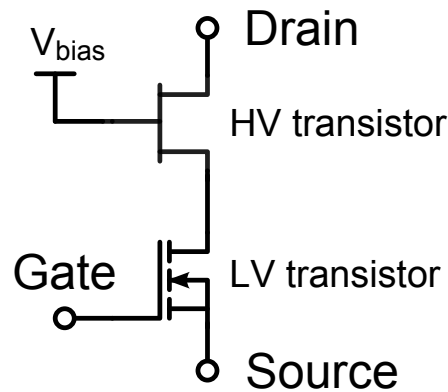


Figure 1.5: A simple cascode circuit

1.3.4 The power cascode

Despite greatly improved performance in comparison to silicon devices, many types of WBG transistor have undesirable driving characteristics, which have the potential to compromise the reliability of a power converter. To increase acceptance of their devices, several manufacturers have therefore promoted the use of the power “cascode” circuit as a way of mitigating the undesirable driving characteristics of their devices, without adversely affecting their switching or on-state performance [22–25].

The power cascode circuit consists of a low voltage MOSFET connected in series with the source of a much higher voltage power transistor. A diagram of a simple cascode circuit is shown in figure 1.5. When the low voltage transistor is switched, the high voltage transistor is also forced to switch, enabling the cascode circuit to behave as a single power device. This arrangement is simple to drive, switches quickly and can be easily customised for a particular application.

Despite its apparent simplicity, the power cascode has yet to gain widespread acceptance, particularly in commercial applications. As will be shown in the following chapter, previous investigations of cascode behaviour have been strongly focussed on specific applications. There is therefore little practical information available for design engineers wishing to implement and optimise WBG cascode switches in general applications. A study of the practical design considerations and trade-offs of the cascode circuit is therefore timely.

1.4 Aims of the work

This work aims to address the practical barriers to the adoption of the cascode circuit as a method of driving WBG power devices. It is intended to provide a clear, concise and application-independent reference of design considerations for any design engineer consid-

ering using a WBG cascode power circuit. Specific consideration is given to the following areas:

- Understanding the benefits and limitations of using cascode circuits to drive WBG devices.
- Explaining the influence of individual circuit and device parameters on switching performance, to allow cascode performance to be optimised by appropriate device selection and control.
- Examining new methods of implementing cascodes to mitigate their disadvantages, maximise their benefits and widen their application to other high voltage (HV) devices.
- Critical examination of relevant previous work reported in the literature by experimental validation of results.
- Considering the practical consequences of applying WBG cascodes to real applications where electromagnetic interference (EMI), isolation and reliability are concerns.

This work focuses specifically on cascode devices with blocking voltages between 600 V and 1200 V. Devices with these ratings are particularly important in electrical power conversion, since they are widely used in grid-level applications. Such applications, which include industrial motor drives, grid connections for renewables and electric vehicles, have some of the greatest potential for improving global energy efficiency. Indeed devices with these blocking voltages account for as much as 78% of the \$4 billion global IGBT market [26, 27].

1.5 Summary of the thesis

The thesis consists of six further chapters:

- Chapter 2 considers the background to the research. Existing silicon devices and their limitations are reviewed, before WBG materials and devices are introduced as alternatives and their characteristics are described. The background and operation of the cascode circuit as a power switch is explained and existing literature on the subject is reviewed. From this, the limitations of previous work are identified and used to inform the direction of the research.
- Chapter 3 describes the experimental methods used, including the design and manufacturing methods used for the experimental set-up and the selection and calibration of test equipment. Specialist measurement techniques required in the work are described in detail and their accuracy validated.

- Chapter 4 explores circuit modelling. A ‘simulation program with integrated circuit emphasis’ (SPICE) sub-circuit model of a SiC vertical JFET is created, using multiple device models to overcome modelling limitations. The JFET model is used to simulate the behaviour of a WBG cascode switching a clamped inductive load. A simplified mathematical model of cascode hard-switching is developed to aid device selection and implementation. Both the SPICE simulations and the mathematical model are validated against experimental measurements.
- Chapter 5 compares the static characteristics of SiC JFETs, SiC MOSFETs and silicon super-junction power devices in a cascode configuration with those of the same devices operating individually. This is used to understand the impact of the cascode circuit on conduction losses. Cascode reverse conduction is investigated as a low loss alternative to external free-wheel diodes and the high temperature behaviour of SiC JFETs and MOSFETs is compared to assess the likely impact of temperature on cascode performance.
- Chapter 6 investigates the dynamic behaviour of cascode circuits and the relative merits of SiC JFETs, SiC MOSFETs and silicon super-junction power devices are compared, both in and out of cascode circuits. The effects of gate resistances and stray inductances are investigated in detail to understand their impact on switching performance. The effectiveness of various methods of $\frac{dV}{dt}$ control are examined, as is the sensitivity of the cascode circuit to spurious turn-on due to voltage transients and its reverse recovery behaviour.
- Chapter 7 concludes the thesis by summarising the findings of the research as a comprehensive design guide for WBG cascode switching circuits. Suggestions for future research directions are also made.

1.6 Contributions

The following original contributions to the field are made in this thesis:

1. The development of an accurate SPICE model of a SiC vertical JFET, accounting for its internal resistance, short-channel effects and voltage-dependent capacitance.
2. The measurement of extreme I-V curves deep into the saturation region of a SiC JFET, allowing accurate characterisation of its short-channel behaviour.

3. The development of a linearised model of cascode switching, enabling simple cascode performance optimisation by parameter inspection.
4. The use of a voltage source HV gate bias to improve static and switching behaviour and experimental validation of its advantages.
5. The use of enhancement-mode WBG devices in cascode configuration to mitigate gate-drive limitations.
6. A direct comparison between individual and cascode on-state and switching behaviour of three distinct devices.
7. Detailed experimental investigation of the role of gate resistance in the control of cascode switching, with separate consideration of low voltage (LV) turn-on, turn-off and HV gate resistors.
8. Experimental measurement of the effect of stray inductance on cascode switching behaviour.
9. Investigation of the use of GaN devices as a LV switch in a WBG cascode circuit.
10. Investigation of the immunity of cascode circuits to spurious turn-on resulting from voltage transients.

Chapter 2

Background

2.1 Introduction

This chapter explores the importance of the WBG cascode circuit and the need to study its design and optimisation if it is to become established in industrial applications. The development and limitations of both silicon and WBG devices are described to explain the problems associated with gate drive and device behaviour that the cascode circuit is able to resolve. The development of the cascode circuit is then described from its origins to its use in silicon-based power electronics. Finally, recent research on WBG cascode circuits is reviewed in detail.

2.2 Modern silicon power devices

Silicon transistors currently dominate power electronic systems except in the highest power applications, for which vacuum tube devices are still sometimes preferred. The fabrication of silicon wafers is an effective mass-manufacturing process, which keeps device costs low and makes device development straightforward. Silicon power devices can be divided into two categories: bipolar and unipolar devices, each of which have specific advantages and disadvantages.

2.2.1 Bipolar devices

Bipolar (minority carrier) devices use both electrons and holes to act as charge carriers. In the on-state, minority carriers are injected into the drift region, where they reach high concentrations. This process is known as conductivity modulation and leads to a significant reduction in apparent on-state resistance, particularly in high-voltage devices. Bipolar devices are char-

acterised by a low forward voltage drop that increases approximately logarithmically with current, making them well-suited to high voltage and high current applications.

The switching speed of bipolar devices is limited because the accumulation and extraction of minority carrier charge at turn-on and turn-off takes a finite time. Bipolar devices therefore tend to suffer from greater switching losses than unipolar devices, making them less suitable for operating at high switching frequencies [28].

The most important silicon bipolar devices in the 600 - 1200 V range are the P-N rectifier diode and the IGBT. Whilst BJTs and thyristors are available at these ratings, they have largely been displaced by the IGBT except in low cost and high current applications respectively.

IGBTs are widely available with ratings into the hundreds of amps [29]. IGBTs combine the simplicity of a MOS gate drive with the low on-state losses of bipolar conduction. Switching losses are typically higher than for equivalent MOSFETs, due to the turn-off “tail current” effect that results from the extraction of minority charge. Nevertheless, switching frequencies approaching 100 kHz are possible with modern high speed trench-stop devices [30]. IGBTs are also well suited to higher temperature applications (100-175 °C), in which they benefit from much more favourable on-state loss temperature coefficients than MOSFETs [31]. They are easily paralleled and are readily available in power modules capable of handling kiloamps. A wide range of off-the-shelf IGBT drivers also makes them easy devices to drive.

Silicon P-N junction diodes are the only form of passive rectifier available in the 600 - 1200 V range and can be capable of conducting thousands of amperes. However, despite the existence of fast and ultra-fast recovery diodes with reverse recovery times of the order of microseconds and hundreds of nanoseconds respectively, their reverse recovery behaviour can result in significant switching losses, especially at high switching frequencies.

2.2.2 Unipolar devices

Unipolar (majority carrier) devices use only one type of charge carrier to conduct current in the on-state. Due to the resistance of the drift region, which tends to increase with blocking voltage, unipolar devices experience an approximately linear relationship between device current and voltage drop for a given gate-source voltage. Unipolar devices therefore tend to experience much greater on-state losses than bipolar devices, particularly at higher currents and voltages. However, the absence of minority carriers in unipolar devices means switching speeds are limited only by device parasitics rather than by minority carrier charge. This means that unipolar devices experience much lower switching losses than bipolar device, making them better suited to high frequency applications.

MOSFETs are the only unipolar silicon power device available in the 600 - 1200 V range and typically have ratings of up to 1 kV and tens of amps [32]. Almost all MOSFETs in this

voltage range are of the ‘super-junction’ type, which have much lower on-state resistance than equivalent conventional planar MOSFETs. However, the switching performance of super-junction MOSFETs is compromised due by the large surface of area of their internal P-N junction diode, which results in a very ‘snappy’ reverse recovery characteristic and increased switching losses [33]. Power MOSFETs are easy to drive, despite sometimes substantial input capacitance and off-the-shelf gate drivers are widely available.

No passive unipolar silicon rectifiers such as Schottky barrier diodes exist in the 600 - 1200 V range, due to the voltage limitations of the silicon Schottky junction.

2.2.3 Limitations of silicon devices

Silicon power device improvements have allowed converter switching frequencies to increase by an order of magnitude per decade over the last 40 years [21]. However, many silicon power devices now operate close to the fundamental material limits of silicon and scope for further improvement is limited.

A solution to this problem is to use alternative semiconductor materials with less restrictive material properties. For example, power devices fabricated from a semiconductor capable of supporting a higher critical electric field than silicon would allow the advantages of unipolar devices to be realised at much higher voltages, since drift regions and hence on-state losses could be made proportionally smaller. In the 600 - 1200 V range, this would allow Schottky diodes to replace P-N diodes and FETs to replace IGBTs. Consequently, device losses in converters could be reduced, improving efficiency and power density. WBG semiconductors are a class of material that meet these requirements.

2.3 Wide bandgap semiconductors

Wide bandgap semiconductors are materials with bandgaps significantly greater than those of silicon (1.1 eV). The two most important WBG semiconductors at present are SiC and GaN, for which commercial devices are now widely available. Research is also ongoing into other materials with even wider bandgaps such as diamond (C) [34, 35] and aluminium nitride (AlN) [36]. However, commercial devices in these materials remain a distant prospect and are likely to target voltages far above the 600 - 1200 V range of interest in this work. They are not considered further herein.

		Si	4H-SiC	GaN
Properties	Bandgap, E_G (eV)	1.1	3.2	3.4
	Relative dielectric constant, ϵ_r	11.7	9.7	9.0
	Electric breakdown field, E_C (kV/cm)	300	3500	3300
	Electron mobility, μ_n (cm ² /V·s)	1400	650	990 (2000)
	Thermal conductivity, λ (W/cm·K)	130	430	130
	Sat. electron drift velocity, v_{sat} ($\times 10^3$ m/s)	100	200	250
	Max. operating temperature, T_{max} (°C)	300	870	500
	Physical stability	Good	Excellent	Good
FOMs	HMFOM (switching performance) = $E_C \sqrt{\mu}$	1.0	7.9	9.3 (13.1)
	HCAFOM (power density) = $\epsilon E_C^2 \sqrt{\mu}$	1.0	77	78 (111)
	HTFOM (thermal capability) = $\frac{\lambda}{\epsilon E_C}$	1.0	0.3	0.1 (0.1)

Table 2.1: Properties and normalised unipolar figures of merit for silicon, SiC and GaN semiconductors. Figures quoted for GaN in brackets account for the enhanced mobility of the 2DEG found in HEMTs. The most desirable values are highlighted in **bold** [37–40]. (Note: Only the 4H-SiC polytype is considered, due to its dominance in the current SiC device market)

2.3.1 Material benefits

The material properties of SiC and GaN are compared with those of silicon in table 2.1. However, material properties alone do not translate directly into power device performance. This problem was addressed by Huang [37], who devised figures of merit for unipolar devices, to allow semiconductor materials to be compared directly, based on their theoretical switching performance, power density and thermal capability. These measures are included in table 2.1.

The most important advantage of WBG semiconductors is their high critical breakdown field (E_C) compared to silicon. This allows the size of drift regions in both SiC and GaN devices to be reduced substantially for a given blocking voltage, which greatly reduces on-state losses. As a result, unipolar WBG devices are feasible at much higher blocking voltages than for silicon. Furthermore, it allows WBG devices to be smaller for a given current rating, which reduces parasitic capacitances and thus reduces switching losses [41]. These switching and power density advantages are readily apparent in the figures of merit of table 2.1.

2.3.2 Comparative device performance

Figure 2.1 shows the theoretical limits of on-state resistance and breakdown voltage for various SiC, GaN and silicon devices. Although silicon IGBT and superjunction MOSFET devices have been able to exceed the theoretical limits of silicon for simple unipolar devices, their performance is already surpassed by unipolar SiC and GaN devices. This demonstrates the

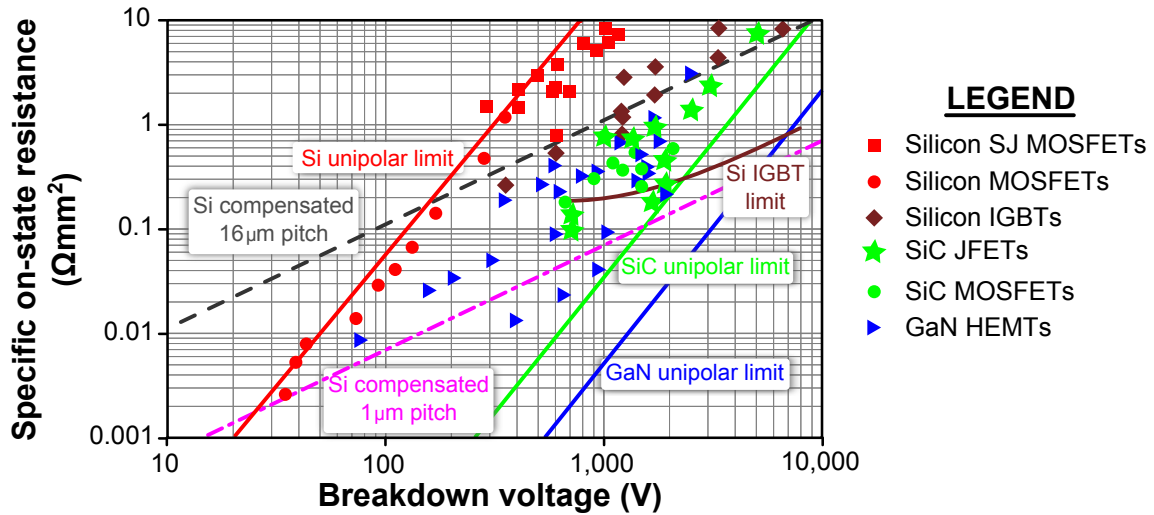


Figure 2.1: Manufactured devices and limits of on-state resistance with blocking voltage for silicon, silicon carbide and gallium nitride [42–44].

ability of WBG semiconductors to extend the advantages of high-speed unipolar transistors to much higher voltages than is currently practicable with silicon. The capability of SiC and GaN devices are compared against existing silicon devices in figure 2.2. This shows how these WBG materials are able to extend converter power ratings and operating frequencies beyond what is possible with silicon devices.

2.3.3 High temperature operation

The high temperature capability of WBG semiconductors was initially of great interest in the literature and it was hoped that high temperature device operation, could be the key to high converter power density. However, other limitations such as device thermal runaway and poor efficiency were shown to limit maximum device temperatures to well below any semiconductor limits [46, 47]. Furthermore, higher temperature operation leads to reduced reliability due to accelerated degradation of components and thermal cycling stresses.

Device operating temperatures much above those possible with silicon ($>175^{\circ}\text{C}$) are therefore generally undesirable in high power density applications and such operating conditions are not considered here. However they do remain of interest for specialist applications.

2.4 Silicon Carbide

Silicon carbide (SiC) is the material of stardust, having been in existence even longer than our solar system [48]. Whilst common in space, its mineral form (*Moissanite*) is exceptionally

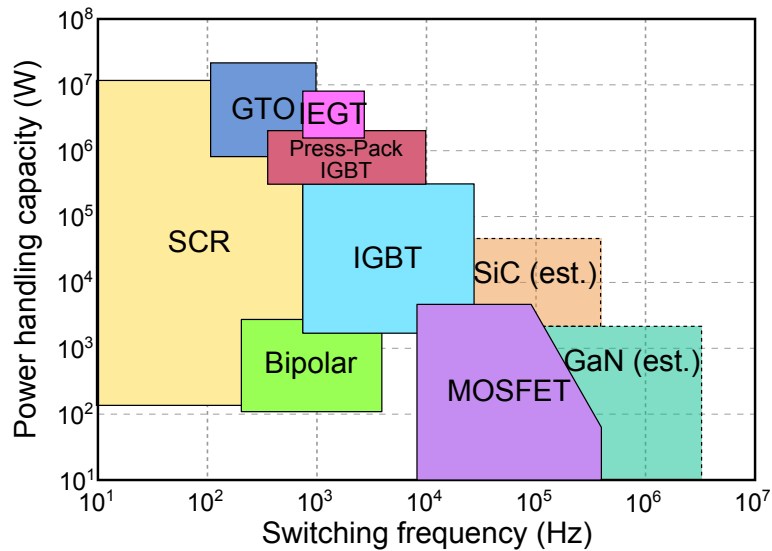


Figure 2.2: Power handling and switching frequency capability of various semiconductor devices [45]



Figure 2.3: Synthetic Moissanite as a diamond substitute in the author's wife's engagement ring. Photograph is by the author.

rare on earth, found only in meteorites, volcanic formations and as inclusions in other minerals [49]. Consequently, all SiC used today is produced synthetically.

2.4.1 Applications

Silicon carbide's strong covalent crystal structure and thermal properties make it ideal for a wide range of applications, particularly as an abrasive and a refractory material [50]. Its hardness and high refractive index also make it an effective diamond substitute for jewellery [51], a fact that has been independently verified by the author (figure 2.3). SiC is also the most mature WBG semiconductor, with power devices having been commercially available since 2002.

2.4.2 Use as a semiconductor

The semiconductor properties of SiC have been known since the early 20th century, having been associated with both the invention of the cat's-whisker detector (a crude form of Schottky diode) in 1906 [52] and the light-emitting diode in 1907 [53]. Although SiC was originally seen as a more promising semiconductor material than silicon [54], it fell out of favour as a result of processing difficulties and the introduction of the Czochralski process for cheaply manufacturing high quality silicon.

Over 100 different crystal structures (polytypes) of silicon carbide exist. However, only one (4H-SiC) is widely used today for power semiconductors, due to its good mobility characteristics and the availability of high quality substrates [55]. Early SiC devices were very expensive due to high material costs. Even so, overall cost savings were possible in certain applications where the excellent electrical performance of SiC devices allowed the size and cost of other components to be reduced [44]. Material costs have since fallen sharply as sales volumes and wafer sizes have increased: by around 85% for SiC Schottky diodes since their introduction in 2002 and around 95% for SiC MOSFETs since their introduction in 2011 [56].

SiC is well suited to high power and high reliability applications. This is partly due to its high thermal conductivity, which enables heat to be effectively removed from device dies. It also possesses excellent physical stability and a reliable native oxide layer. Its coefficient of thermal expansion is also well matched to a range of ceramic substrates often used for high power packaging [35]. This makes it a desirable material for power modules and some commercial ceramic packaged examples exist [57].

There are currently two mature SiC switching devices available: MOSFETs and JFETs.

2.4.3 SiC MOSFETs

SiC MOSFETs have been commercially available since 2011 [58] and are currently available with ratings of up to 1700 V and 60 A [59]. Their low gate charge and much lower drain-gate (Miller) capacitance than any other SiC device permits very rapid voltage switching. In conjunction with their low on-state resistance and high voltage rating, this makes SiC MOSFETs attractive devices for high power density applications. All SiC MOSFETs are normally-off (enhancement-mode) devices, which is advantageous in most power converter topologies; in the event of gate driver power failure, the device will fail safe. The structure of a typical SiC MOSFET is shown in figure 2.4.

Early MOSFETs suffered from unreliability associated with the SiO₂ gate oxide. This has mostly been resolved in commercial devices through improved processing such as nitridation of the SiO₂ interface [62]. Modern devices claim reliabilities equivalent to or better than HV

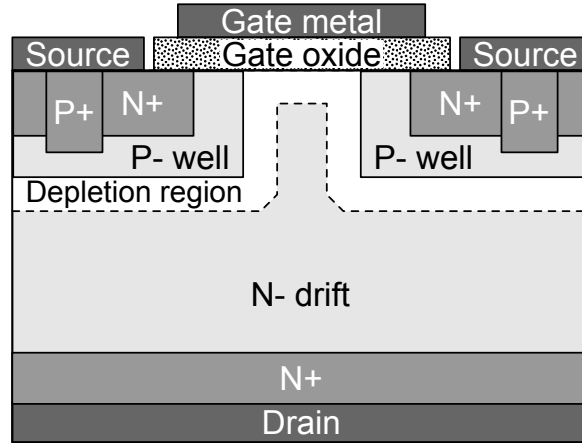


Figure 2.4: Typical structure of a SiC MOSFET [60, 61]

silicon MOSFETs [63]. However, the inversion layer below the gate oxide suffers from low mobility [64], resulting in poor transconductance, a higher specific $R_{DS(ON)}$ compared to SiC JFETs and a need for substantial gate drive voltages.

The low channel mobility and the presence of trapped charge at the interface between the channel and the SiO_2 gate insulator leads to unusual high temperature behaviour in SiC MOSFETs [65]. Normally, high temperatures are associated with increased on-state resistance as a result of phonon scattering reducing mobility. However, SiC MOSFETs initially experience a slight decrease in on-state resistance with rising temperature, due to their interface charge [65]. This makes paralleled SiC MOSFETs susceptible to uneven current distribution. Additionally, the SiC MOSFET threshold voltage is temperature dependent and falls with increasing temperature [66].

Despite its normally-off behaviour, SiC MOSFET gate drive is not as straightforward as for silicon transistors. Due to its low transconductance, the MOSFET requires a gate voltage of at least 20 V to fully enhance its channel. This is within 5 V of the rated breakdown voltage of the gate oxide layer and leaves little margin to cope with voltage transients. Furthermore, the decrease in threshold voltage with temperature makes SiC MOSFETs susceptible to spurious turn-on at elevated temperatures. A negative turn-off voltage is therefore recommended by device manufacturers to mitigate this [67].

2.4.4 SiC JFETs

Normally-on (depletion mode) vertical JFETs are the most mature SiC transistors, having been available commercially since 2005 [68]. Modern commercial SiC JFETs use vertical structures, which minimise on-state resistance at the expense of slightly higher gate charge compared to lateral devices [69]. These parts operate close to the theoretical limits of current

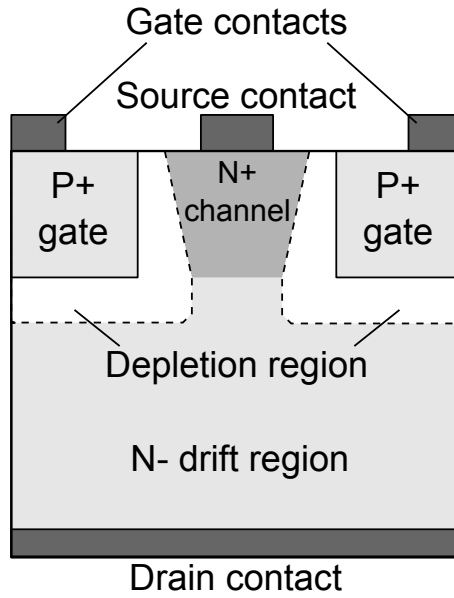


Figure 2.5: Structure of SiC vertical JFET [64]

density for unipolar SiC transistors [70] and are expected to be preferable to bipolar SiC devices at up to at least 3 kV [71]. The structure of a typical vertical power JFET is shown in figure 2.5.

The JFET is a voltage controlled device. In a normally-on device, a zero or slight positive bias (<2.5 V) is required to fully-enhance the channel and turn the JFET on, whilst to turn it off, a negative bias of a few volts is required to pinch-off the channel. There is typically some variation in pinch-off voltages between JFETs and it is also temperature dependent [72]. Gate biases larger than around +2.5 V and -15 V are generally undesirable since they cause gate-source diode forward conduction and avalanche breakdown respectively. Whilst not necessarily damaging to the device, overdriving the gate in this way unnecessarily increases gate drive losses.

2.4.4.1 Benefits

Unlike most FETs, SiC vertical JFETs have negligible drain-source capacitance and no intrinsic body diode [73, 74]. Their input capacitance is also low compared to similarly rated SiC MOSFETs. Reverse conduction is possible through the channel and the absence of both drain-source capacitance and a body diode leads to negligible reverse recovery losses [75].

SiC vertical JFETs are well suited to high reliability applications. Their simple structure precludes the presence of any intrinsic parasitic devices that could cause latch-up and contains no gate oxide layers that could degrade or be damaged by transients [76]. Device breakdown occurs only by an avalanche mechanism. This is non-destructive, provided the

energy dissipated is limited [71]. Indeed, due to their high temperature capabilities and the uniform channel current distribution that arises from a positive channel resistance temperature coefficient, SiC JFETs can handle large avalanche and short-circuit currents without damage [76]. This makes them ideal for circuit protection applications and high current ratings can be achieved by simply connecting multiple devices in parallel [77].

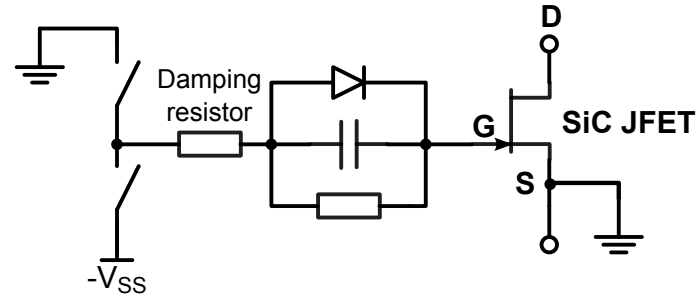
2.4.4.2 Gate drive

The gate drive of JFETs has long been of concern. As depletion-mode devices, JFETs requires a negative gate voltage to switch them off. Should the gate driver ever be unpowered, as is the case under start-up conditions or if the gate drive power supply fails, the JFET uncontrollably conducts current, potentially destroying both it and the converter. JFET gate drive is also complicated by its gate diode characteristic: pinch-off voltages are variable and the margin between this and the gate-source breakdown voltage can be small. The situation is complicated further if a positive gate voltage is used to minimise on-state losses [64]. These gate drive limitations have been a major barrier to widespread acceptance of the SiC JFET.

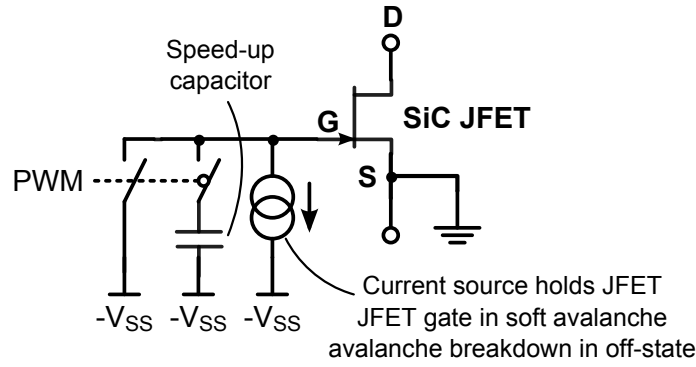
Several attempts have been made to mitigate these concerns. Semisouth, a former manufacturer of SiC JFETs were able to produce a range of “normally-off” JFETs by adjusting the width and doping of the device channel to raise the pinch-off voltage above 0 V [78]. Despite being genuine enhancement-mode switches, normally-off JFETs were substantially compromised compared to normally-on JFETs: the low threshold voltage puts the transistor at risk of spurious turn-on unless a negative turn-off voltage was used, whilst the devices’ input capacitance and on-state resistance were significantly higher than for depletion mode devices. Furthermore, normally-off JFETs were only fully enhanced when their gate-source diode was heavily forward biased and conducting at least half an amp, resulting in significant gate drive losses [79, 80]. Normally-off JFETs have not been available since the closure of Semisouth in 2012.

A variety of gate drive circuits have been proposed to account for difficult JFET gate characteristics. Elegant solutions were proposed by Domes and Round [77, 81], both of whom proposed methods that held the JFET gate in soft avalanche breakdown in the off-state (figure 2.6). These approaches were most valuable with early JFETs, which had widely variable pinch-off characteristics. However, neither scheme addressed the undesirable depletion-mode JFET characteristics.

As a result of the undesirable depletion-mode and gate drive characteristics, cascode circuits have been used widely to drive normally-on JFETs [22, 76, 82]. The cascode circuit avoids many of the disadvantages of normally-off JFETs and of alternative gate drive designs. The development of the SiC JFET cascode is described in detail in section 2.8.1.



(a) Round's gate drive



(b) Domes' gate drive

Figure 2.6: Gate drive methods proposed by Domes and Round for SiC JFETs [77, 81]

2.4.5 BJTs

BJTs are the only other SiC device of relevance to the 600 - 1200 V range. However, development lags behind both the SiC JFET and MOSFET, although commercial devices have recently become available. Despite some attractive properties, the use of SiC BJTs is hampered by their substantial base current requirements which arise from their low gain [83]. It therefore seems unlikely that SiC BJTs will be able to compete against two mature devices that are already produced commercially in high volumes.

2.5 Gallium Nitride

2.5.1 Background

Gallium nitride was conceived in 1969 as a semiconductor to allow the development of blue LEDs [84]. The first efficient blue LED was eventually realised using GaN in the 1990s, winning its creators the Nobel Prize [85]. GaN transistors have since become established in radio frequency (RF) applications, where their high mobility and saturated electron velocity

make them well suited to high-frequency operation [55]. The use of GaN in power electronics is more recent, with commercial power transistors becoming available in 2009.

2.5.2 Materials properties

Bulk GaN wafers are not currently manufactured commercially due to material quality issues, although this may change in the medium term [86]. Current GaN power devices are therefore fabricated on silicon or SiC substrates instead. GaN transistors on silicon can be closely integrated with drive circuitry and are inexpensive due to the low cost of silicon. Although the cost of processing individual GaN on silicon wafers is slightly higher than for pure silicon, the high power densities possible with GaN mean that individual GaN on silicon devices are now cheaper than their silicon counterparts [87]. GaN on SiC devices are significantly more expensive due to the high cost of the SiC substrate and to date, no GaN on SiC devices are commercially available.

2.5.3 GaN HEMTS

GaN possesses the exceptionally useful ability to form heterojunctions. This allows it to be used to make high electron mobility transistors HEMTs, in which a high concentration of electrons is confined in a two-dimensional sheet with very high mobility. In GaN power HEMTs, the channel electron mobility is almost double that of the bulk mobility (see figures in brackets in table 2.1).

GaN HEMTs therefore exhibit very low on-state resistance and can operate with current densities at least 10 times higher than those of silicon devices [88]. In turn, this makes GaN HEMTs very fast switching devices, since these high current densities allow device dies to be small and minimises parasitic capacitance.

A basic structure for a typical GaN HEMT is shown in figure 2.7.

2.5.3.1 Commercial devices

Several commercial GaN HEMT power transistors are now available. The most mature devices are EPC's range of enhancement-mode 'eGaN' devices with voltage ratings of between 40 and 200 V. Recently, 600 V devices have become available from companies including Transphorm and International Rectifier (now Infineon) [90]. Although marketed as normally-off devices, these high voltage transistors are actually depletion mode HEMTs, in a cascode configuration with a normally-off silicon MOSFET. Research devices with much higher blocking voltages have also been reported [91], but these remain some way from commercialisation.

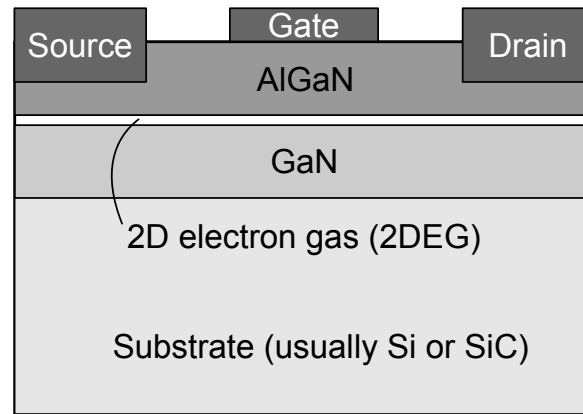


Figure 2.7: Basic structure of a typical GaN HEMT [89]

2.5.3.2 Reliability

GaN on silicon devices suffer from several limitations that raise concerns about reliability, including a high degree of lattice mismatch between layers, different coefficients of thermal expansion, poor thermal performance, lateral channels and high field strengths [92].

In GaN HEMTs, breakdown behaviour is a particular concern. Unlike SiC JFETs, several drain-source breakdown mechanisms exist and drain leakage current can be significant at high voltages [93]. Due to the presence of the 2DEG under the gate, many devices are unable to prevent avalanche currents flowing into the gate, with serious implications for the gate driver [44]. GaN HEMT gate junctions are also extremely sensitive to avalanche currents and even modest gate overvoltages can damage the device.

Naturally, manufacturers are happy to claim these reliability concerns have been overcome [87] and the fact that some GaN devices now meet JEDEC reliability standards partially supports this [94]. However, recent publications [93, 95] make it clear that concerns about GaN reliability have yet to be completely resolved and widespread industrial acceptance of GaN devices may therefore still take some years to achieve.

2.5.3.3 Gate drive

Driving normally-on GaN HEMTs poses similar problems to those of SiC JFETs. Whilst enhancement-mode HEMTs are possible, their on-state resistance and gate voltage margins are degraded. As a solution to this problem, manufacturers of GaN HEMTs now offer 'normally-off' GaN devices consisting of a normally-on GaN HEMT in a cascode arrangement with a silicon MOSFET.

2.5.4 Other devices

It is likely that HEMTs will remain as the only commercially available GaN power devices for the foreseeable future. GaN MOSFETs are difficult to manufacture due to the lack of a native insulating semiconductor oxide, whilst GaN BJTs are impractical due to very short carrier lifetimes. GaN Schottky diodes are technically feasible, but are unable to compete against lower cost SiC Schottky diodes, which are a mature technology with very similar characteristics [44].

2.6 WBG device selection

The ‘best’ choice of WBG semiconductor is strongly application dependent. For grid-level applications, the properties of GaN make it an excellent choice for integrated high switching frequency applications below 1 kilovolt and a few tens of amps. GaN HEMTs are a likely candidate for displacing silicon superjunction MOSFETs. In contrast, SiC devices are well suited to applications requiring higher voltages, currents and temperatures, making them an obvious choice for high power modules and a promising silicon IGBT replacement.

The SiC MOSFET, SiC JFET and GaN HEMT all suffer from gate characteristics that make them harder to drive than silicon devices. A number of manufacturers have suggested the cascode circuit as a way of mitigating the normally-on characteristics of some of these devices. However, the cascode is also capable of addressing other problems associated with these devices such as poor transconductance, low threshold voltages and gate junction breakdown. In the following section, the background of the cascode circuit and its application to WBG power electronics is reviewed.

2.7 The cascode circuit

2.7.1 Theory of operation of the power cascode

The power cascode consists of a LV transistor with its drain connected to the source of a HV power transistor as in figure 2.8. The LV transistor is therefore able to impose a voltage between the gate and source of the HV transistor, thereby controlling its switching. Its operation is described briefly here, but is reviewed in detail in chapter 4.

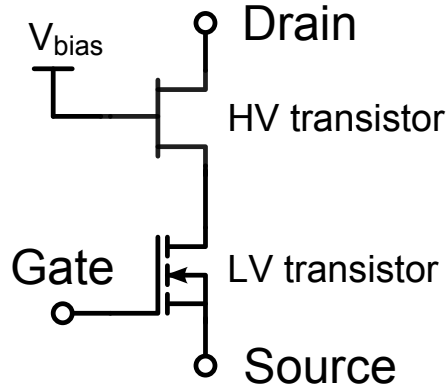


Figure 2.8: A power cascode circuit

2.7.1.1 Turn-on

Before turn-on, the gate of the LV transistor is held below its threshold voltage by the gate driver, allowing it to support a voltage between its drain and source ($V_{DS(LV,off)}$). The HV gate is held at a constant bias (V_{bias}) so that in the off state, the HV gate-source voltage is below its threshold voltage and equal to $V_{bias} - V_{DS(LV,off)}$. The HV device therefore blocks the entire voltage, less $V_{DS(LV,off)}$.

When the LV transistor's gate is driven above its threshold voltage, it switches on, causing $V_{DS(LV)}$ to fall to zero. As a result, the HV gate-source voltage rises quickly past its threshold voltage to V_{bias} and the HV transistor switches on, causing it to stop blocking voltage and start conducting current. The cascode is now in the on-state and its total resistance is the sum of the on-state resistances of the two transistors.

2.7.1.2 Turn-off

Turn-off starts when the gate of the LV transistor is driven below its threshold voltage, causing the transistor to start to turn off and $V_{DS(LV)}$ to increase. Rising $V_{DS(LV)}$ causes the HV gate-source voltage to drop until its threshold voltage is reached. At this point, the HV transistor voltage rises until it is blocking the entire voltage, less $V_{DS(LV)}$. This prevents $V_{DS(LV)}$ rising further and limits the voltage across the LV transistor to a few tens of volts, even if the HV transistor is blocking substantially greater voltages. The cascode drain current falls to zero and it is now fully switched off.

2.7.2 Invention of the cascode and use as an amplifier

The cascode circuit was first described in 1939 by Hunt and Hickman who used two triode valves connected in cascode in a voltage stabiliser circuit [96]. The high frequency benefits

of the circuit were first demonstrated by Wallman et al. in 1948 [97]. Here, it was shown that a pair of cascoded triode valves were able to match the excellent frequency response of a pentode valve, whilst exhibiting a much better noise figure. The cascode amplifier has such good high frequency characteristics because of the common-base connection of the upper transistor. Any Miller current arising from changes in voltage across the cascode is shunted directly to small-signal ground, thereby eliminating the Miller effect and giving a wide device bandwidth.

The triode valve cascode amplifier was quickly adopted for RF applications, notably television. Its excellent low noise performance and high gain made it an ideal choice as a front-end amplifier and its advantages quickly became widely known [98].

The solid-state cascode appeared in the mid 1960s - some time after the invention of the transistor. This was possibly due to the initially poor high frequency performance of transistors compared to thermionic valves. The gain and stability of the cascode were particular attractions, as was the possibility of using two low cost transistors in cascode configuration to exceed the high frequency performance of an expensive high-end device [99]. Both BJTs and FETs were used in the cascode configuration around this time, despite the much greater maturity of BJT devices at this stage [100].

With the development of integrated circuits in the late 1960s, cascode circuits became recognised as a cost effective way of improving the gain and voltage ratings of transistors within integrated circuits. By 1968, the monolithic cascode had made its commercial debut in the LM102 voltage follower [101].

The cascode amplifier has remained a fundamental building block of RF amplifiers ever since, being described by Horowitz and Hill [102] as “the famous cascode configuration”. It is widely used today in radio ICs such as Bluetooth receivers [103], wireless LAN receivers [104] and even in EHF applications into the hundreds of gigahertz [105].

2.7.3 The silicon power cascode

The power cascode circuit was first reported in a patent filed by Baliga in 1981 and published in 1987 [106]. This detailed the use of a low voltage normally-off transistor such as a MOSFET or BJT to control a normally-on HV device such as a field-controlled thyristor (FCT) or a JFET as shown in figure 2.9. The patent describes the cascode as a way of using depletion-mode devices in an enhancement mode configuration, but also acknowledges its high turn-off gain and high $\frac{dV}{dt}$ and $\frac{dI}{dt}$ capability.

The cascode fitted well with the prevailing interest in combinations of bipolar and FET technology [107], particularly given the early commercialisation of IGBTs that was occurring at around the same time. It was particularly attractive as a way of simplifying the otherwise

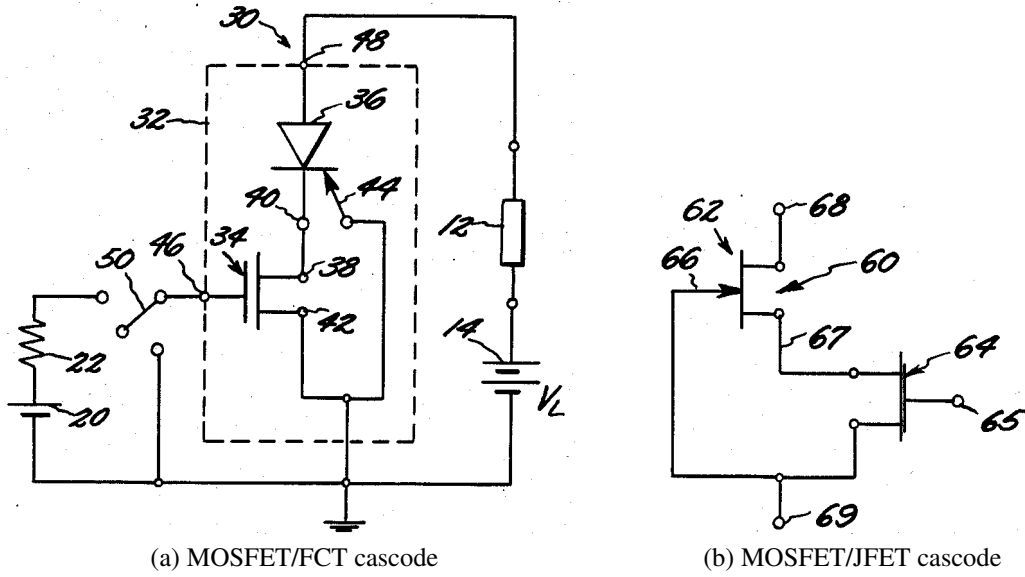


Figure 2.9: Original drawings for MOSFET-controlled power cascodes from Baliga's 1987 patent [106].

challenging drive requirements of HV BJTs, as well as for its rapid turn-off speed and hence potential for high frequency operation.

A particularly promising application was the gate turn-off (GTO) thyristor cascode, which was expected to offer high voltage (>1000 V) and current ratings at what would then have been high switching frequencies of 20 - 100 kHz [108, 109]. This was of particular interest, since contemporary BJTs were not available in ratings above 1,500 V and additionally suffered from poor current gain. However, within a few years, IGBTs with these ratings were readily available and interest in thyristor cascodes diminished.

In the last few years, there has been some renewed interest in silicon power cascodes, as IGBT technology has matured, BJT development has continued and 'super-junction' MOSFETs have appeared [110]. One notable development was the monolithic MOSFET-BJT cascode, known as the 'emitter switched bipolar transistor' (ESBT), which claimed to have superior high frequency performance in comparison to IGBTs [111, 112]. Whilst ST Microelectronics produced these devices commercially, they have never gained a large market share, not least due to their limited current ratings of up to 3 A. The advantages of these devices have now been superseded by both WBG devices and more recent IGBT designs. At the time of writing, commercial ESBTs were "not recommended for new designs" [113].

An alternative approach was taken by Broadmeadow et al, who investigated using superjunction MOSFETs in a cascode configuration; the first time a power cascode using two enhancement-mode MOSFETs has been reported [114, 115]. Although this concept is in-

teresting, these studies are limited as they only investigate the turn-on process and not the considerably more complex turn-off process.

Whilst silicon power cascodes continue to generate some interest in the literature, the maturity of other silicon power devices and the emergence of WBG devices have all but eliminated their benefits. However, it is clear from these previous studies that cascode circuits are a practical way of driving devices with excellent conduction and switching behaviour but otherwise inconvenient gate characteristics.

2.8 The wide bandgap cascode

2.8.1 Invention and promotion by manufacturers

The WBG cascode originated at around the same time as the SiC JFET, in the early 2000s [116]. Realising that customers would be wary of using depletion-mode devices in power converters, semiconductor companies manufacturing SiC JFETs promoted their use in a cascode configuration to broaden their appeal. SiCED, a spin-off from Siemens/Infineon was the first to capitalise on this approach, and even producing a co-packaged SiC JFET/Si MOSFET to simplify implementation [82].

2.8.1.1 Developments with SiC

This trend was continued by Semisouth, who patented the concept of a fully-SiC integrated cascode [117]. This used a low voltage enhancement-mode JFET to drive a high voltage depletion-mode JFET and was intended for high-temperature operation. A similar idea was also described by McNutt et al. [118].

Semisouth, in conjunction with Alpha and Omega Semiconductor, were also the first to suggest the use of a ‘stack cascode’ in 2012 [119]. In this design, SiC JFET and Si MOSFET dice are laid directly on top of each other to reduce parasitic inductance, as shown in figure 2.10. This approach was claimed to provide exceptionally low gate charge and on-state resistance and much higher power density, even compared to competing SiC MOSFETs. Although the closure of Semisouth in 2012 meant that this design was never commercially realised, it has since been investigated further by United Silicon Carbide who report slightly improved switching behaviour using the concept [23].

Further refinements of the SiC cascode have been reported by United SiC, who patented a method of manipulating the pinch-off of a HV JFET and providing separate turn-on and turn-off HV gate resistances to maximise turn-on speed [120]. This is an important development because cascode turn-on is usually much slower than turn-off. Significantly, United SiC has

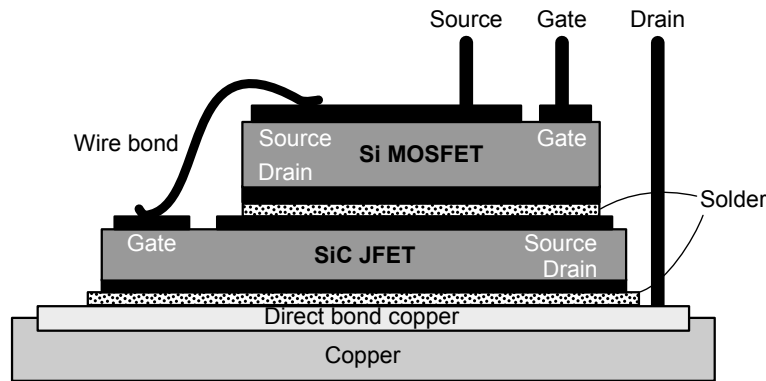


Figure 2.10: The ‘stack cascode’ concept [76]

also been able to demonstrate that SiC JFET cascodes are as robust as standalone JFETs under short-circuit and avalanche conditions [23], making SiC JFET cascodes particularly useful for applications such as solid-state circuit breakers.

2.8.1.2 Developments with GaN

The emergence of GaN devices has seen continued interest in cascode circuits. Manufacturers such as Transphorm/Fujitsu and International Rectifier/Infineon are now developing or commercially selling integrated GaN cascodes which use an enhancement mode Si MOSFET to drive a depletion mode GaN HEMT [24, 25, 121]. As with SiC JFETs, normally-off variants of GaN HEMTs exist, but suffer from limited threshold voltages, restrictive maximum gate voltages and increased device capacitances. [122]

It is telling that, despite the existence of enhancement-mode variants of typically depletion-mode devices, the cascode circuit continues to be promoted by manufacturers. Despite their slightly higher on-state losses compared to individual transistors, cascode circuits benefit from straightforward gate drive and fast switching. In contrast, normally-off GaN HEMTs and SiC JFETs experience degraded switching and gate drive performance, in addition to higher on-state losses.

2.8.2 Practical considerations

2.8.2.1 Comparative studies

Comparative studies between the performance of standalone SiC JFETs and SiC JFET cascodes have been conducted by Singh and Rodriguez-Alonso et al. [82, 123]. In general, cascode switching losses were found to be of similar magnitude to those of an individual JFET, although Rodriguez-Alonso showed there was also a clear dependence on the converter mode of

operation. However, Rodriguez-Alonso did not ensure that the cascode and individual JFETs were subjected to equal drive levels in the on-state, with individual JFETs driven to +2 V and cascoded JFETs driven to 0 V. This suggests that the cascode circuit could perform slightly better than reported, if on-state drive levels were matched.

2.8.2.2 Device protection

The avoidance of avalanche breakdown during switching has been investigated in several publications. It is a concern because during the final stages of cascode turn-off, a redistribution of charge between the LV output capacitance and HV gate-source capacitance causes a step change in HV source voltage. This process is described in detail in section 4.9. In some situations, this can cause drain-source breakdown of the LV device or gate-source breakdown of the HV device. Such behaviour causes undesirable switching losses and may affect reliability.

LV device breakdown has been reported as a particular problem with GaN HEMT cascodes, possibly as a result of their comparatively high output capacitance [124]. Although described as being caused by a ‘capacitance mismatch’ between the HV and LV devices, it is more generally due to a ‘switching speed mismatch’ caused by the LV device switching off much faster than the HV device. It could feasibly be corrected by careful choice of LV MOSFET drain-source capacitance, increasing the turn-off gate resistance, or by increasing the LV MOSFET output capacitance.

Two patented methods for avoiding LV device breakdown are the addition of capacitance in parallel with the LV output capacitance [125] and clamping the HV gate-source voltage [126]. However, the novelty of the latter patent is questionable, with the concept having been described somewhat earlier by Semisouth [22].

2.8.2.3 Soft-switching operation

The use of GaN cascode switches in zero-voltage switching (ZVS) topologies has attracted significant interest [127, 128]. These topologies take advantage of the fact that the cascode turn-off process is much faster than turn-on. Losses can therefore be minimised by only hard-switching the cascode at turn-off, whilst soft-switching it at turn-on.

This technique only works with specific topologies and places limitations on the operating mode, for example by requiring critical conduction mode (CrM) operation in a boost converter. Additionally, the turn-on process is somewhat different to that of a hard-switched cascode and it becomes very important to match the switching speeds of the HV and LV devices. It has been shown that these device matching issues can cause losses to occur within the HV device

during turn-on, even if drain-source voltage measurements for the entire cascode suggest zero voltage switching [128].

Losses due to mismatched devices can be reduced by increasing the size of either the HV gate-source capacitance or the LV drain-source capacitance, although the benefits of doing so are tempered by a slight increase in turn-off losses [124, 129].

2.8.2.4 Packaging

The emergence of extremely fast switching GaN cascodes has led some authors to investigate the effect of packaging on cascode performance. The ‘stack’ cascode approach invented by Semisouth has therefore also been applied to GaN cascodes as a way of reducing stray inductance [130]. A further development is the inclusion of gate drive ‘Kelvin’ connections in cascode packages, which avoids problems with ‘ground bounce’ resulting from the exceptionally high $\frac{dI}{dt}$ possible with these circuits. This concept is particularly important, since it eliminates the effects of the LV source inductance which would otherwise significantly limit cascode switching performance [131, 132].

2.8.3 Circuit variations

2.8.3.1 Capacitor-clamped cascode

Only one technique in the literature, known as the ‘capacitor-clamped cascode’, truly addresses the asymmetry between cascode turn-on and turn-off, without adversely affecting turn-off speed [133]. Rather than the HV gate being connected directly to ground, it is instead connected via a capacitor. The gate is protected by a voltage clamp to ensure its rated voltage is not exceeded. This arrangement is shown in figure 2.11.

At turn-off, Miller current flowing through $C_{DG(HV)}$ charges this capacitor, causing a significant voltage to build up at the HV gate. The cascode is nevertheless able to switch off, albeit slightly more slowly than usual, since the voltage across the LV transistor also increases to compensate.

At turn-on, the high HV gate voltage causes drain current to rise rapidly, by forcing a rapid transition through the HV device’s transfer characteristic and by imposing a large voltage across any stray source inductance. Reverse conduction behaviour also benefits, since the JFET channel can be nearly fully enhanced with only a small reverse voltage, if a Zener diode is used to protect the gate [134].

Although promoted by Semisouth in a product demonstration board [22], the capacitor-clamped cascode has several drawbacks. The size of the clamp capacitor is critical and optimum values vary between devices and applications. If it is too small, the HV device becomes

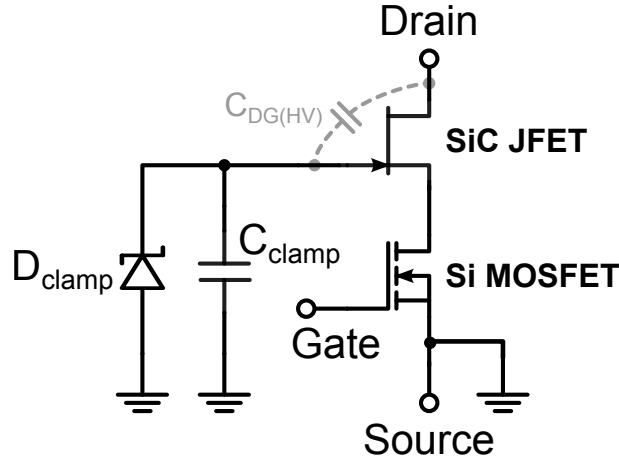


Figure 2.11: The capacitor-clamped cascode concept [133]

very sensitive to spurious turn-on from external $\frac{dV}{dt}$ and accumulated charge is easily dissipated by leakage currents. If it is too large, the Miller current is unable to impose any significant change in gate voltage and the benefit of the arrangement is lost. Turn-off losses can also be expected to increase slightly, although the reduction in turn-on losses is usually much greater.

There are also reliability concerns, since this approach specifically reduces the robustness of the cascode circuit to $\frac{dV}{dt}$ transients (discussed in chapter 6.7). Additionally, its safe use is probably restricted to JFETs and BJTs, rather than devices with delicate gates such as MOSFETs and HEMTS, so that any excess charge can be harmlessly dissipated into the semiconductor bulk.

2.8.3.2 Reverse conduction

A ‘synchronous’ cascode reverse conduction mechanism has been reported by both Sheridan and Domes, although neither author has quantified its performance compared to discrete diodes [73, 135]. Under reverse bias, as soon as the LV transistor reverse body diode conducts, $V_{GS(HV)}$ is clamped such that the HV transistor is switched fully on. Reverse conduction therefore occurs through the LV body diode and the HV channel. However, Domes also reported excessive turn-on reverse recovery losses in cascode bridge circuits, due to the presence of the additional device capacitance of the LV transistor.

Although greater reverse recovery losses might be anticipated in a cascode circuit, the losses reported by Domes are much higher than would be expected given the size of the extra capacitance. It is also at odds with the low loss reverse recovery behaviour described by other authors using different devices [121, 122]. Due to the widespread use of reverse conduction mechanisms, it is important that this claim is experimentally verified. This is done in section 6.8.

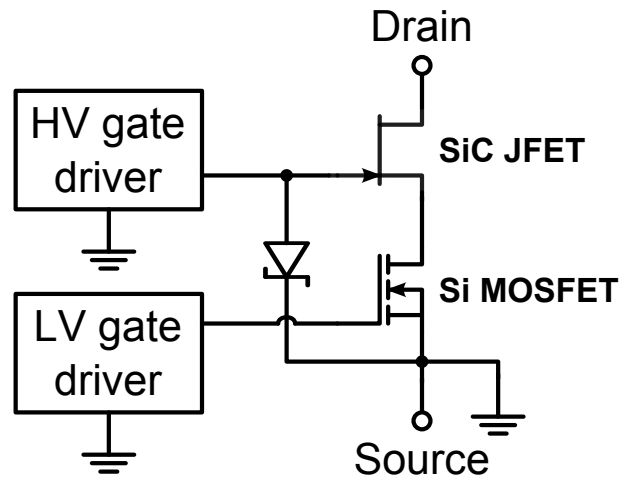


Figure 2.12: The ‘cascode light’ configuration [135].

2.8.3.3 ‘Cascode light’

To address the apparent problem with bridge circuits, Domes proposed a concept called ‘cascode light’. This used a dedicated gate driver to hold the LV MOSFET permanently in the on-state, whilst the HV device is switched with an independent gate signal. This arrangement is shown in figure 2.12.

Under normal conditions, reverse recovery losses are eliminated by removing the LV MOSFET from the switching process. However if the gate drive power supply fails, the LV MOSFET defaults to the off-state, safely disabling the cascode. This approach was promoted by Infineon who marketed a complete system of gate drivers, LV MOSFETs and SiC JFETs based on the idea [136]. However, the product line seems to have since been quietly dropped, with no products having been available since its announcement in 2012.

An alternative approach was described by Guédon et al. [137], which used a capacitor charged by the gate driver to hold a JFET cascode in the off-state in the event of power failure. However, the design was extremely complex and flawed, such that the JFET gate junction would unintentionally be held in deep avalanche in the off-state.

There is little convincing evidence that the benefits of the ‘cascode light’ outweigh its complexity. However, the concerns raised by Domes require investigation to determine whether cascode circuits are appropriate in bridge converter topologies.

2.8.4 Analytical studies

2.8.4.1 Modelling

Despite widespread interest in cascode circuits, attempts to model their operation have been surprisingly limited. Whilst numerous authors have modelled devices frequently used in cascode circuits [64, 138] and carrier-level simulations [139] of cascodes have been developed, there are few examples of circuit-level mathematical models of the cascode switching process. A complete circuit-level model is particularly helpful for designing practical circuits, as it provides an insight into how component selection influences circuit behaviour.

Various aspects of the circuit-level behaviour of cascodes during switching have been described by Roig [140], Siemienieć [141], Aggeler [142] and Rodriguez-Alonso [123]. However, Roig and Aggeler consider only the switching behaviour of the circuit in the context of long term reliability and $\frac{dV}{dt}$ control respectively. Rodriguez-Alonso provides detailed equivalent circuits for stages of switching, but stops short of developing a complete model.

Siemienieć provided a more complete analysis of cascode switching, notably considering the effect of adding gate resistance to the HV device as a means of improving stability. However, this analysis is not worked through to form a complete mathematical model, although useful analyses of the controllability and stability of the switching process are provided.

Unfortunately, Siemienieć's analysis of cascode turn-on suffers because of his assertions that full control over the turn-on process is only possible if the LV device is turned on slowly and that turn-on $\frac{dV}{dt}$ and $\frac{dI}{dt}$ transients can be controlled using a large gate resistor. Although these assertions are partially true, there are many practical examples of cascode circuits that have already been described here, which turn on safely without large gate resistors. Furthermore, limiting turn-on $\frac{dV}{dt}$ and $\frac{dI}{dt}$ transients is known to excessively increase switching losses [143].

The most comprehensive circuit model of cascode switching has been developed by Huang et al. to describe the switching process in a GaN cascode [144]. The level of detail included in this model enables very precise predictions of performance to be made for a given set of operating conditions. However, the complexity of the derived equations (described in the Laplace domain) makes it impossible to interpret the effects of circuit by simple inspection of variables. This severely limits the use of this model for cascode design and optimisation.

It is also interesting that both Huang and Rodriguez-Alonso choose to neglect the effects of HV device gate resistance in the control of cascode turn-off $\frac{dv}{dt}$ and instead model the rise in $V_{DS(casc)}$ as a capacitive charging process. Even in the absence of an external HV gate resistor, it is common for HV WBG devices to have internal gate resistances of several ohms

[79, 145], which suggests this voltage rise should more accurately be modelled as being Miller current limited.

Finally, it is surprising that no analysis of the cascode considers the possibility of a gate bias other than 0 V being applied to the HV transistor gate. This precludes the application of cascode switches to enhancement-mode power devices.

2.8.5 Applications

WBG cascodes have been reported in a variety of applications, but there is scant evidence of any commercial use. The applications investigated in the literature reflect the cascode's specific advantages, particularly its fast turn-off transient and normally-off behaviour. Consequently, almost all of these involve hard-switched turn-off and voltage-source converters, with high power density grid interfaces and motor drives attracting the most interest [122, 146–148].

A novel approach to grid interfacing using WBG cascode devices was reported by Vasquez et al. [149] who used a SiC JFET cascode as a passive synchronous rectifier by substituting the LV transistor for a silicon Schottky diode. Despite some reverse recovery current, losses were still lower than for conventional silicon rectifier diodes. At the other end of the frequency scale, the emergence of GaN cascodes has extended interest in the cascode to high frequency ZVS resonant circuits, where its high turn-off speed is particularly valuable. [127].

Cascode circuits have also been investigated as a way of switching very high voltages. By using a WBG cascode-driven HV cascode circuit or 'super cascode', the possibility of switching several kilovolts in a few tens of nanoseconds has been demonstrated [150, 151], with possible applications in pulsed-power and perhaps also grid interconnections.

2.9 Conclusion

It is clear from this review that interest in WBG cascodes is widespread and likely to grow, particularly as commercial depletion-mode and cascode WBG devices become more widely available. Even if effective enhancement-mode alternatives to existing depletion-mode devices emerge, there will continue to be applications where cascode circuits are advantageous. For example, in robust solid-state SiC JFET based circuit breakers, or perhaps as a way of driving the first generation of diamond transistor devices when they are developed.

WBG cascodes continue to struggle to be accepted in commercial products, which may be partly due to concerns about the reliability of WBG devices themselves. However, there is also a lack of information for design engineers who might otherwise consider using the

circuit. Much of the literature is strongly focussed on specific applications and practical design techniques for WBG cascodes are rarely discussed.

This thesis addresses this problem by examining aspects of the design and optimisation of the cascode circuit that are important for it to be used effectively in real circuits, but are widely overlooked in the literature. The conclusion of this work is then intended to act as a design reference for anyone wishing to take advantage of this useful circuit.

Chapter 3

Experimental techniques

3.1 Introduction

This chapter examines the experimental techniques used in the following experimental work. It explains the reasons for the choice of experimental methods and equipment used as well as the design process for the test printed circuit boards (PCBs) and experimental set-up.

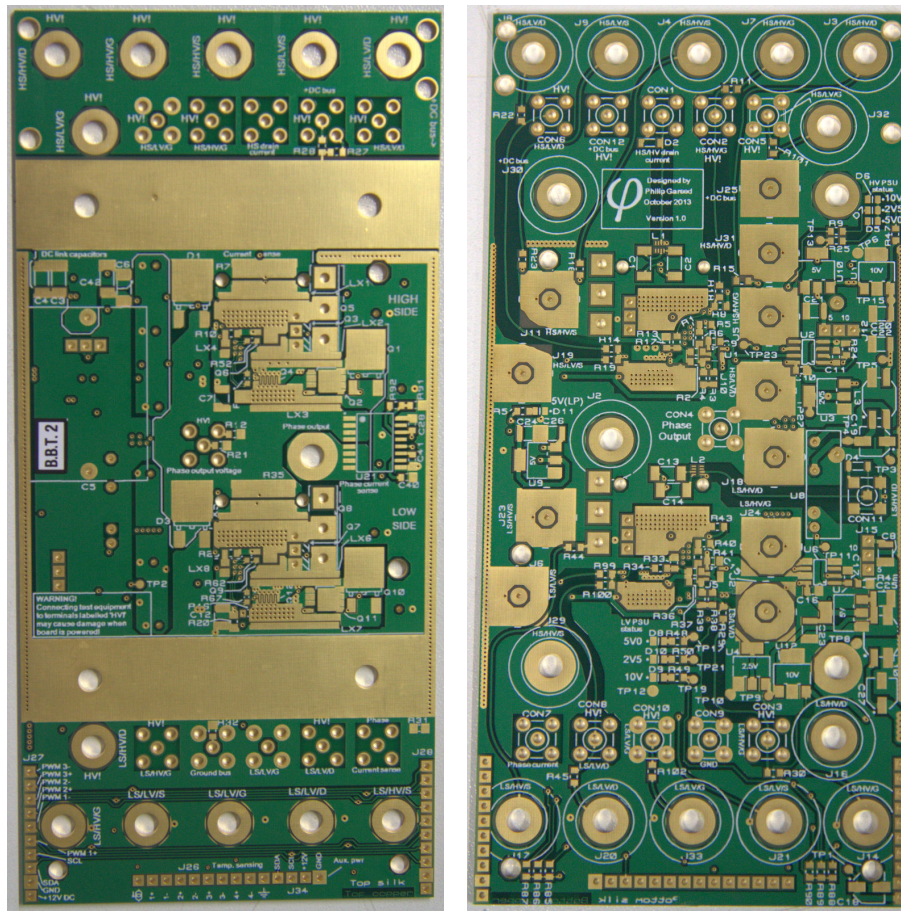
The limitations of the test and measurement methods used are discussed in detail and quantified. Where necessary, the technical background to these limitations and the experimental approaches used to overcome them are described. The calibration techniques used to ensure confidence in the experimental measurements are also explained.

3.2 Test PCB

High-frequency circuits are very sensitive to variations in layout, hence for consistency between experiments it is desirable to use a single test PCB. The PCB used in this work was designed to allow *in situ* static and dynamic measurements to be made for a variety of transistors operating both individually and in a cascode configuration (figure 3.1). Measurement connections were built into the PCB and careful consideration given to the layout to minimise ground loops and EMI. The PCB also included the facility to add inductance at several points in the cascode circuit to allow the effect of stray inductance to be investigated.

3.2.1 Design of the PCB

Detailed schematics and layout drawings of the 4 layer test PCB are shown in appendix C. The key design features are described below:



(a) High voltage side

(b) Control side

Figure 3.1: A bare test PCB

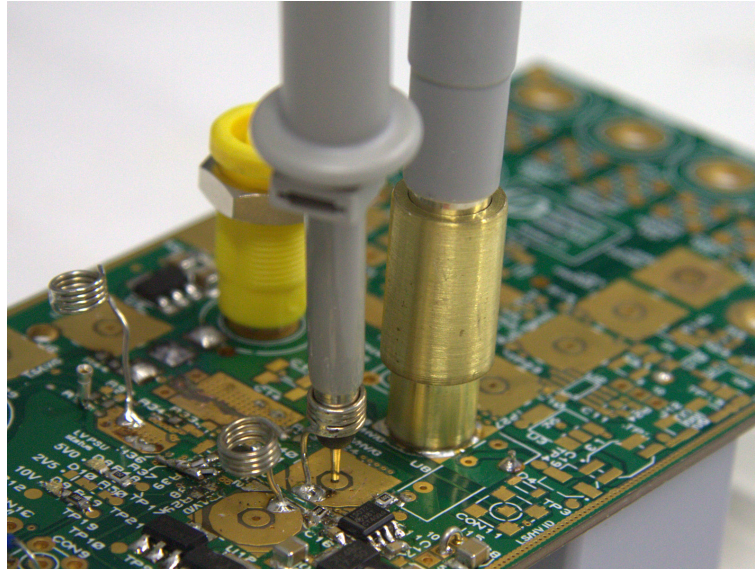


Figure 3.2: Grounding methods for different passive voltage probes. LV passive probe grounding spring is on the left-hand side, HV passive probe brass sheath is on the right-hand side.

3.2.1.1 Oscilloscope probes connections

Measurements from oscilloscope probes are vulnerable to spurious interference due to the high $\frac{dV}{dt}$ expected in WBG and cascode switching circuits. This high-frequency interference can be minimised by ensuring that the loop formed by the probe tip connection to the PCB and the ground reference connection is as small as possible.

Probe connections to the PCB were made by direct connection of the probe tip to the PCB, on the opposite side to the power tracks. Coupling from electrically noisy parts of the circuit to the oscilloscope probes was therefore minimised by the shielding effect of the internal ground planes of the PCB.

Each probe test point was surrounded by a grounded region connected directly to the internal ground plane. For the LV probes, this connection was made using a grounding spring soldered directly to the PCB. For the HV probes, a custom-made brass sheath was used, ensuring complete shielding of the probe tip from spurious $\frac{dV}{dt}$ interference. These grounding methods are shown in figure 3.2.

Occasionally, high frequency ringing was observed in measurements due to parasitic oscillations coupling into the oscilloscope probes. This was eliminated where necessary using a toroidal ferrite core as a common-mode choke to damp the ringing in the probe cable without unduly limiting bandwidth.

3.2.1.2 Curve tracer/resistance measurement connections

The PCB included traces to permit *in situ* measurements of static device performance using a curve tracer or precision multimeter. This enabled Kelvin connections to be made directly to the drain, gate and source of both the HV and LV transistors of both the upper and lower switches, to give greatly enhanced accuracy for low-impedance measurements.

These measurement traces included a zero-ohm resistor close to their connection point to the power circuit, allowing these traces to be disconnected from the circuit when switching measurements were being made. This eliminated the possibility of additional interference or parasitic effects being caused by their presence.

Under some circumstances, the lack of gate resistance in the curve tracer circuits led to oscillatory effects and misleading measurements when using the Kelvin measurement traces. Under these circumstances, sufficient damping resistance was added in series with the gate connection to eliminate the parasitic oscillations. The size of the damping resistance was selected to be large enough to damp the oscillations, but small enough to avoid adversely affecting switching speed. Since the curve tracer used operates with a measurement period of around 200 μs , only extremely large values of gate damping resistance would compromise measurement accuracy.

3.2.1.3 Current measurement loop

Direct measurements of device drain current were made using a Rogowski coil. To allow the Rogowski coil to completely enclose the current path, a copper measurement loop soldered across a break in the drain track was used. Its inductance was minimised by fabricating it from a flat conductor wide enough to span the width of the drain track as shown in figure 3.3. The additional inductance of the current measurement loop was found by experiment to be of the order of 0.1 - 0.4 nH, using the method described in section 3.8.

3.2.1.4 Additional inductance

Thin breaks were included in the power tracks at the HV drain, gate and source as well as the LV source. This made it possible to add additional inductance to the power traces in these locations, to investigate its effect on switching behaviour. Off-the-shelf commercial air-core surface-mount device (SMD) inductors were used for this purpose, for the tight tolerances and repeatability they offer. They are described in detail in section 3.8.11.

When not required, these breaks in the PCB tracks were short-circuited using copper tape of the same width as the track, soldered across the gap. The inductance of a flat inductance

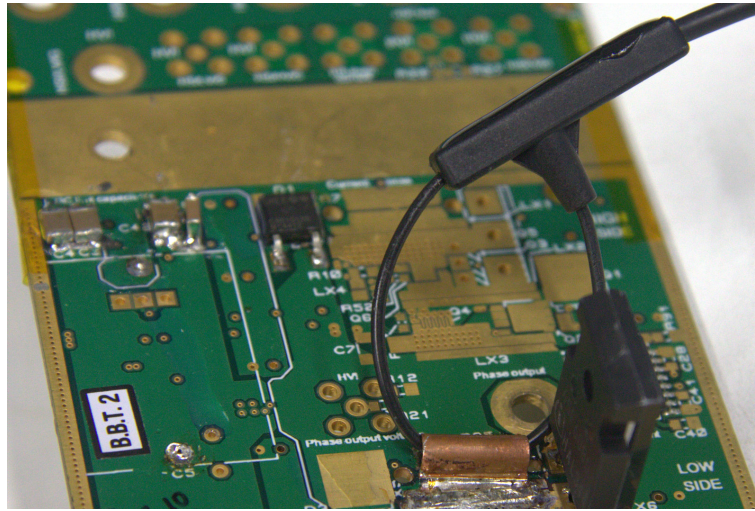


Figure 3.3: Copper measurement loop and Rogowski coil

is largely insensitive to its thickness [152], so this method caused minimal variation between measurements.

3.2.1.5 Power supplies

Low-voltage power to the PCB was supplied from an isolated 12 V DC laboratory power supply, referenced to the 0 V bus. The power supplies to the upper and lower switches were referenced relative to the upper LV transistor source and 0 V bus respectively. Power to the upper switch was supplied through a galvanically isolated 12 V - 12 V integrated DC switching regulator.

The power supply outputs for the entire PCB and both the upper and lower switches were filtered by a large common mode choke. Low equivalent series resistance (ESR) ceramic decoupling capacitors were used throughout the PCB, to minimise conducted emissions. The gate driver and HV gate bias power supplies for both switches were supplied directly from separate linear regulators with an input ripple rejection ratio of around 48 dB at 100 kHz [153].

These measures ensured a consistent power supply to both switches during operations and minimised common-mode interference which could affect circuit performance.

3.2.1.6 EMI considerations

Proper control of EMI is important to avoid unintentional coupling causing parasitic oscillations or corruption of voltage or current measurements. Layout is therefore an important design consideration.

Coupling of transients into sensitive sub-circuits was minimised by keeping connections as short as possible and by minimising the loop inductance of signal paths. The impedance of ground connections was kept as low as possible through the use of a continuous ground plane, to reduce the likelihood of transient effects such as ‘ground bounce’. This ground plane in the middle layers of the PCB also provided effective shielding between the high voltage traces on one side of the board and the low voltage traces on the other.

3.2.1.7 Spacing

To minimise the inductance of the PCB traces, track spacings were reduced to close to the minimum recommended creepage distances for the voltages used. To reduce the possibility of arcing between tracks or board layers due to either electric field concentration at track edges or by transient over-voltages, a high dielectric strength conformal coat was applied over sections of the PCB expected to experience more than 100 V.

3.2.1.8 Power transistor connections

To allow testing of transistors in a variety of packages, several footprints were included for both the HV and LV transistors. For the HV transistor, footprints for a bare die, TO-220 and TO-247 package were included, whilst for the LV transistors, footprints for a 200 μm pitch ‘bumped die’, power quad flat no-lead (PQFN) and TO-252 package were included. Emphasis was placed on minimising the inductance of the the connections to the lowest inductance packages.

3.2.2 Die attach process

In some experiments, the inductance of the cascode circuits needed to be minimised to properly study the effects of gate resistances and stray inductance. To do this, a bare die HV Semisouth SJDP120R085 SiC JFET was used in a cascode configuration with a LV bumped die EPC2015 eGaN FET.

The drain of the bare die JFET was mounted directly to the PCB using a thin layer of soft die attach solder. Gate and source connections were then made by ultrasonic wedge bonding 25 μm gold wire to the source and gate pads at a PCB temperature of approximately 150 °C. Each 1 mm long wire bond had an estimated resistance of 50 m Ω , hence multiple wire bonds were necessary to cope with the large rated current of the JFET. At the source, 22 parallel wire bonds were used to give an overall bond resistance of around 2 m Ω , whilst three parallel wire bonds were used at the gate to give an overall bond resistance of approximately 17 m Ω (figure 3.4).

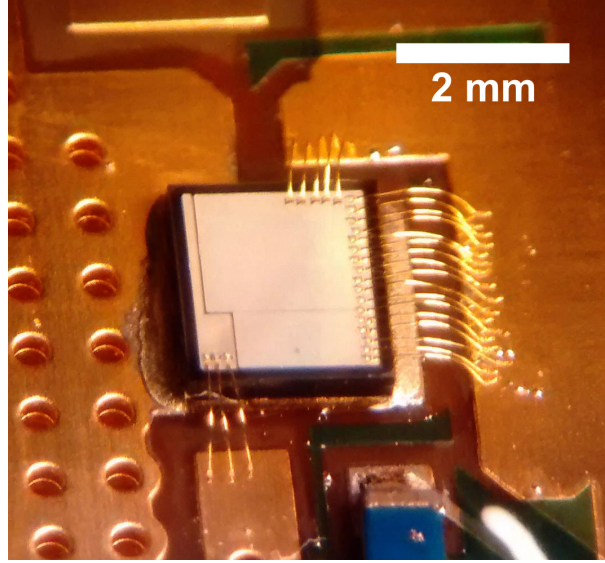


Figure 3.4: Wire bonds at JFET die gate (bottom left) and source (right and top), before encapsulation

The source bond resistance was therefore small compared to the JFET $R_{DS(ON)}$ of approximately $80\text{ m}\Omega$, whilst the gate bond resistance was small compared to the JFET internal gate resistance of $5\text{ }\Omega$.

3.2.2.1 Bond wire inductance

Bond wire inductance can also be minimised using many parallel connections. Measurement of the inductance of bond wires is challenging, but a good estimate may be found from widely available formulae, which assume high frequency operation and non-magnetic materials [152, 154]:

Calculating the individual self inductance of individual round bond wires and treating them as independent parallel inductances will give a lower bound estimate for total bond wire inductance. In reality, the close proximity of the bond wires means their magnetic fields will interact and total inductance will be higher than predicted. The total inductance in nanohenries of n parallel-connected individual round bond wires of radius r mm and length l mm may be calculated using equation 3.1:

$$L_{(\text{round wire})} = \frac{0.2l}{n} \left[\ln \left(\frac{2l}{r} \right) - 1 \right] \quad (3.1)$$

An upper bound estimate of bond wire inductance can be made by assuming that the line of bond wires behaves like a thin flat conductor with a width equal to the distance between the first and last connections. In practice, overall inductance is lower than this, as the separation

	Parallel round bond wires (no mutual inductance) $l = 1, r = 0.0125$		Flat conductor (large mutual inductance) $l = 1, t = 0.025$
Gate ($n = 3,$ $w = 0.25$)	0.27 nH	$\leq L_{G(HV)} \leq$	0.51 nH
Source ($n = 22,$ $w = 2.5$)	0.04 nH	$\leq L_{S(HV)} \leq$	0.17 nH

Table 3.1: Estimated bounds for bond wire inductance.

between bond wires reduces the mutual inductance of the current paths. The inductance in nanohenries of a flat conductor of length l mm, thickness t mm and width w mm can be calculated using equation 3.2.

$$L_{(\text{flat wire})} = 0.2l \left[\ln \left(\frac{2l}{w+t} \right) + \frac{1}{2} + 0.2235 \left(\frac{w+t}{l} \right) \right] \quad (3.2)$$

Using these equations, the range of values within which the gate and source bond wire inductance are expected to fall are given in table 3.1. These estimates support the assumption that bond wire inductance is negligible compared to that of the PCB tracks (measured to be of the order of 5 nH in most cases).

3.2.2.2 Die protection

To protect the die from damage during handling, it was encased in a low-viscosity epoxy resin and allowed to cure.

3.3 Clamped inductive load

3.3.1 Test circuit

Hard-switching waveforms for the devices under test were measured using a clamped inductive load as shown in figure 3.5. This approach was used to replicate switching stresses experienced by power devices operating in hard-switched topologies. Energy loss measurements from a clamped inductive load test can be used to simply estimate switching losses in a hard-switched converter and also give a consistent method of comparing switching performance between devices.

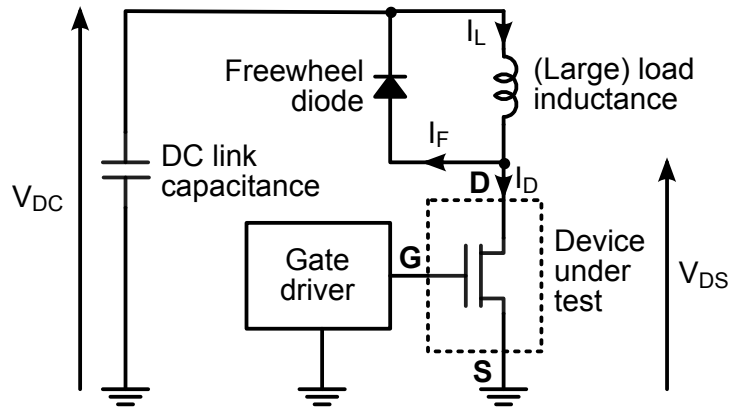


Figure 3.5: Diagram of clamped inductive test circuit

3.3.2 Gate driver

Gate signals to drive the clamped inductive load were generated by a Microchip PIC30F2020 microcontroller on a Microstick II development board. Firmware was written to allow the user to specify the switching current, DC bus voltage and inductor size. These values were used to calculate the required output pulse to switch the test device on for long enough for its drain current to reach the required value, before switching it off for 200 ns, on for 200 ns and finally off. This set-up allowed measurement of both turn-on and turn-off transients under identical conditions to be made. The firmware used is shown in appendix D.

The test PCB was isolated from the PIC microcontroller using an ISO721 opto-isolator with a high (50 GV/s) transient isolation rating. To avoid problems with ground loops, the microcontroller circuit was powered from the universal serial bus (USB), whilst the isolated output connected to the test PCB was powered independently from an isolated DC power supply.

3.3.3 Power inductor

The air-core power inductor was formed from 52 turns of 400 strand 50 μm Litz wire for excellent high frequency performance. It can be seen on the right hand side of figure 3.6. The inductor was wound in a single layer coil on a plastic former, with a length of 103 mm and a diameter of 75 mm. A machined spiral groove ensured there was a small gap between turns, minimising the inter-turn capacitance, to maximise the inductor's self-resonant frequency. Measured with an inductance-capacitance-resistance (LCR) meter at 1 kHz, the power inductor was measured to have an inductance of 102.7 μH and a DC resistance of 0.32 Ω . The self-resonant frequency of the inductor was measured to be 2.7 MHz.

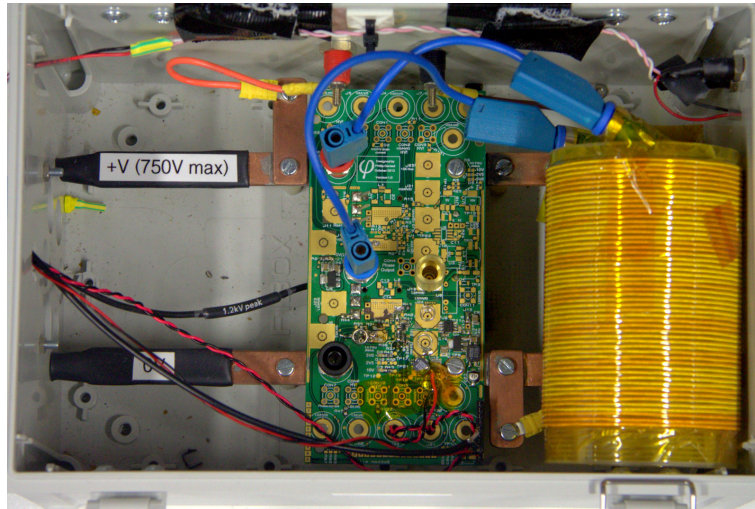


Figure 3.6: Test set-up for clamped inductive load

3.3.4 Free-wheel diode

A Cree C4D10120E SiC Schottky diode rated at 1200 V and 33 A at room temperature was used as a free-wheel diode. By using a Schottky barrier diode, reverse recovery effects were minimised, both due to its lack of carrier recombination and comparatively small capacitance (<100 pF) over the majority of its voltage range [155].

The diode used was packaged in a TO-252 surface mount power package to minimise inductance in the free-wheel loop.

3.4 Test set-up

The clamped inductive load test set-up was enclosed in a polycarbonate box to ensure safe operation. Test PCBs were mounted directly onto copper bus bars inside this box and connections made to the power inductor signal inputs. Measurements of voltage and current were made directly using the oscilloscope probes as previously described. The test set-up is shown in figure 3.6.

3.5 Curve tracing

3.5.1 Tektronix 371A curve tracer

Static device characteristics were measured using a curve tracer. In most cases, a Tektronix 371 A curve tracer was used. This instrument is capable of characterising semiconductors

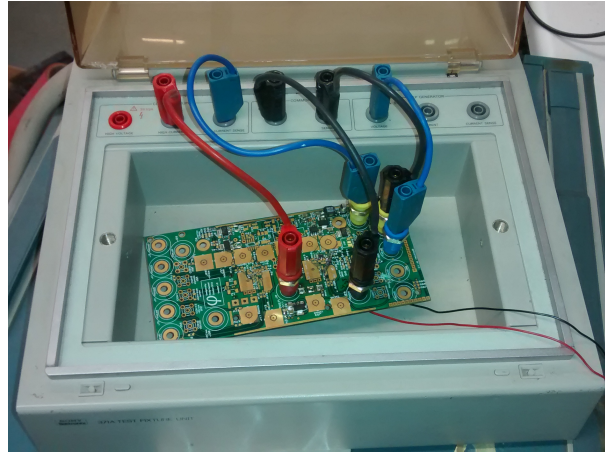


Figure 3.7: Measurement of Si SJ cascode I-V characteristic using Tektronix 371A curve tracer

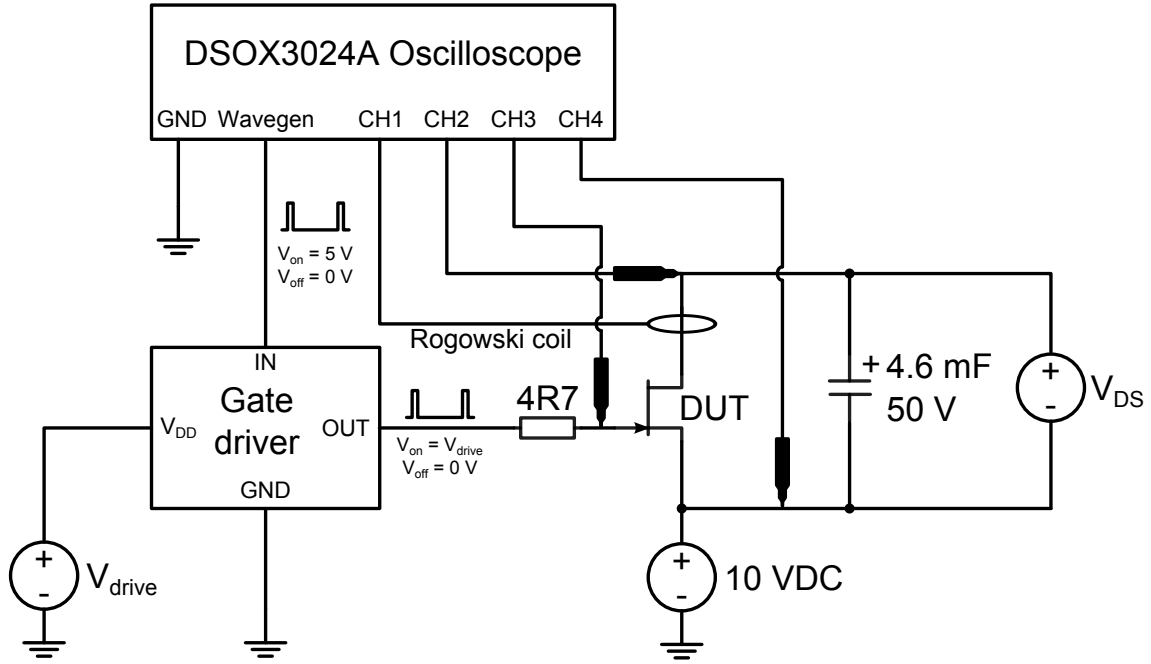
at voltages up to 3 kV, currents up to 400 A and instantaneous powers up to 3 kW [156]. Kelvin connections were used to ensure voltage measurement accuracy, even in low impedance circuits.

By appropriate selection of settings and device connections, this instrument was used to measure device breakdown voltages, I-V curves, transistor or diode forward and reverse conduction characteristics, transistor transfer characteristics and on-state resistances. Due to the limitations of the data analysis tools available on the curve tracer, measurement data were extracted and processed externally. In some cases it was necessary to combine the results of several measurements to cover the ranges of interest. Figure 3.7 shows the curve tracer being used to measure the I-V characteristic of a Si super-junction (SJ) MOSFET based cascode.

A limitation of the Tektronix 371A curve tracer is its comparatively long measurement period, of the order of $200\ \mu\text{s}$. For most measurements, this is not a problem. However, when making measurements far into the saturation region of the SiC JFET, as described in section 4.4.3, self-heating becomes a significant problem and an alternative approach is required.

3.5.2 Custom curve-tracing set-up

A custom curve-tracing set-up was used to avoid problems with device self-heating. This used a much shorter pulse width to ensure that device self-heating was negligible, even at high instantaneous powers. The test set-up is illustrated in figure 3.8.



N.B. Integrator circuit for Rogowski probe and local passive voltage probe grounding are not represented on this diagram

Figure 3.8: Arrangement of short pulse-width curve tracing set-up

3.5.2.1 Drain-source decoupling capacitance

In a conventional curve tracer, long measurement periods are necessary to allow transients to settle after measurement pulses are applied to the device. To make it practical to use very short measurement periods, a large, local, extremely low ESR drain-source decoupling capacitance with high current capability is required. This was fabricated using $10 \times 10 \mu\text{F}$ 50 V X7S ceramic capacitors, $5 \times 100 \mu\text{F}$ 50 V polymer electrolytic capacitors and $4 \times 1000 \mu\text{F}$ 50 V electrolytic capacitors connected in parallel.

This capacitor bank was designed to be capable of supplying up to 50 A continuously for $5 \mu\text{s}$ with a voltage drop of less than 0.1 V, thus eliminating the need for a high current V_{DS} supply. A very low high-frequency impedance was ensured by using flat copper sheet to connect the capacitor bank to the drain and source of the device under test.

3.5.2.2 Gate drive

Gate drive pulses of $5 \mu\text{s}$ width and a frequency of 2 Hz were generated by the on-board signal generator of an Agilent DSOX3024A oscilloscope. $5 \mu\text{s}$ was chosen as the minimum on-time that yielded a stable measurement period for all values of V_{GS} and V_{DS} . These were used to drive a MOSFET gate driver.

The gate driver was powered by a variable DC supply, allowing gate pulses of arbitrary magnitude to be applied to the JFET. By using a $5\ \mu\text{s}$ pulse width, self heating effects were reduced by 97 % compared to using a conventional curve tracer, whilst the 2 Hz measurement frequency ensured a maximum average device power dissipation of the order of 10 mW, even at extreme values of I_D and V_{DS} .

Due to the depletion-mode characteristics of the JFET, a negative gate voltage is required to turn off the transistor. This was provided by a DC bias voltage of 10 V between the source of the JFET and the ground reference of the gate driver circuit. Since the gate driver was not isolated and the signal generator and inputs share a common earth-reference ground connection, it was necessary to use the same ground connection for the passive voltage probes. The resulting 10 V offset in voltage measurements was removed using the oscilloscope MATH function.

3.5.2.3 Measurement method

JFET drain current was measured using a PEM CWT1 Ultra-mini Rogowski current probe. To minimise overshoot or ringing in the current and voltage waveforms, a $4.7\ \Omega$ gate resistor was used, to produce an over-damped response.

Measurements of I_D for several values of V_{GS} were taken by varying V_{DS} between 0 and 30 V at intervals of approximately 0.5 V for $V_{DS} < 5\ \text{V}$ and at intervals of approximately 1 V for $V_{DS} \geq 5\ \text{V}$. Each reading was performed by taking the average value of each parameter over the period between $2\ \mu\text{s}$ and $4\ \mu\text{s}$ after the device was turned on. This aided repeatability by avoiding the point at turn-on where readings were prone to transients and by averaging out any remnant ringing during the measurement period.

For each value of V_{GS} and V_{DS} , the measured value was then obtained by averaging over 10 readings to minimise measurement noise.

3.6 Oscilloscope and probe selection

Appropriate selection of oscilloscope and measurement probes is important for accurate and safe measurement of circuit quantities. Of particular relevance for the measurement of high voltage, fast switching power electronics circuits are the bandwidth, rise time, peak input capability and impedance of each probe.

3.6.1 Oscilloscope

An Agilent DSOX3024A 4 channel, 200 MHz oscilloscope was used in this work. It is particularly important that the oscilloscope is capable of detecting signals with the rise times expected. The shortest rise time detectable by an oscilloscope with an approximately Gaussian response can be shown to be $t_{rise(min)} = \frac{0.35}{f_{BW}}$ [157]. From the simulations carried out in section 6.3.3.1, it is known that the minimum expected rise time is approximately 10 ns for voltage signals and 15 ns for current signals. The DSOX3024A has a rise time specification of ≤ 1.75 ns, which is adequate for this purpose

3.6.2 Probe selection

3.6.2.1 Voltage

Different probes were used to measure the various circuit voltages and these are listed alongside their electrical properties in table 3.2. Only passive single-ended voltage probes were used, which are inconvenient for measuring differential voltages in the presence of a large common-mode component. However, differential voltage probes were not available with both sufficient bandwidth and voltage rating.

The LV passive probes were used for the measurement of low side gate voltages, $V_{DS(LV)}$ and input drive signals. The HV passive probes were used for measurement of high-side voltage, DC bus voltage and $V_{DS(casc)}$.

3.6.2.2 Current

Current was measured using a CWT1 ultra-mini Rogowski coil from Power Electronic Measurements Ltd. (PEM). This has the advantage of flexibility, as the thin coil may be clipped around almost any conductor. However, its bandwidth is limited and its minimum rise time is close to that expected in this circuit. Despite these drawbacks, this was the best current measurement technique available that met the test requirements.

Conventional current probes such as the Agilent N2783B offer greater bandwidth, but are only rated at 300 V relative to earth. Due to their size, including slots in a PCB to permit their use would have also significantly increased circuit inductance [158].

Resistive current sensing is also possible. Coaxial shunt resistors use field-cancelling techniques to achieve bandwidths into the GHz. However, they are physically very bulky, which makes them inflexible and impractical here, where minimising stray inductance is a priority. Coaxial shunt resistors are also generally not isolated, which is problematic for measuring drain currents.

Probe ID	Probe type	Colour code	Sensitivity	Model number
#1	LV passive	Yellow	0.1 V/V	Agilent N2863B
#2		Green		
#3		Blue		
#4		Pink		
#5	HV passive	Yellow	0.01 V/V	Agilent 10076B
#6		Green		
#7	Rogowski coil	N/A	0.02 V/A	PEM CWT1

Probe ID	Bandwidth	Rise time	Peak input	Load on circuit
#1	300 MHz	1.16 ns	>400 V	10 M Ω , ~15 pF
#2				
#3				
#4				
#5	250 MHz	1.4 ns	4,000 V	66.7 M Ω , ~3 pF
#6				
#7	30 MHz	11.6 ns	1200 V, 300 A	~ few pH

(a) Probe electrical specifications

Table 3.2: Properties of oscilloscope probes used in this work [159, 160].

3.6.3 Probe calibration

Each probe has slightly different performance characteristics which must be accounted for if measurements are to be accurate. All the probes used were calibrated and compensated before use and could therefore be expected to operate within their specification.

The ‘skew’ of the probe however, must be calibrated separately. Probe skew occurs when the signal being measured is delayed between the probe tip and oscilloscope. This delay may be as a result of transmission line effects or the signal conditioning circuitry in the probe. If left uncorrected, significant errors may result, particularly in the calculation of switching losses.

3.6.3.1 Voltage probe skew correction

To measure probe skew for the passive voltage probes, each probe was connected to the built-in oscilloscope signal generator, set to output a 10 MHz, 50% duty cycle square wave. The trace from each probe was compared to a reference probe measuring the same signal and the

skew compensation found by adjusting the skew settings for the probe under test until the positive- and negative-going transitions for each waveform were precisely aligned.

3.6.3.2 Rogowski coil skew correction

To measure the skew for the Rogowski coil, a SiC MOSFET cascode (as described in chapters 5 and 6) was used to switch 600 V across a 25 Ω resistive load for approximately 750 ns. To minimise inductive effects, the load was fabricated from four parallel-connected, wide 1210, 100 Ω surface mount resistors. These were connected to the cascode drain by soldering one terminal to the test PCB. The other resistor terminal was soldered to a wide metal strip connected to the DC bus. The inductance of such a large resistive load was therefore negligible compared to its resistance within the oscilloscope bandwidth.

$V_{DS(casc)}$ was measured using a HV passive probe at the cascode drain. The oscilloscope MATH function was used to calculate the voltage across the resistive load by subtracting $V_{DS(casc)}$ from 600 V. Current in the load resistance was measured using a Rogowski coil enclosing the wide metal strip connecting the load resistors to the DC bus. By measuring current around a conductor at a constant potential of V_{DC} , the measurement problems associated with the Rogowski coil $\frac{dV}{dt}$ sensitivity (described in section 3.7) were avoided. These current measurements could therefore be used to calculate the voltage across the load by multiplying them by the 25 Ω load resistance.

An excellent match between the voltage and current-derived measurements was achieved when a current skew of +17.0 ns was applied to the Rogowski coil input, as shown in figure 3.9. These measurements also increase confidence in the ability of the Rogowski coil to accurately measure currents with frequency components approaching its rated bandwidth. Aside from a small amount of parasitic oscillation, there is negligible difference between the voltage and current derived measurements, even with a current transient exceeding 1 GA/s, with rise-times of the order of 20 ns.

3.6.3.3 Skew correction summary

The skew corrections applied to the oscilloscope probes are summarised in table 3.3.

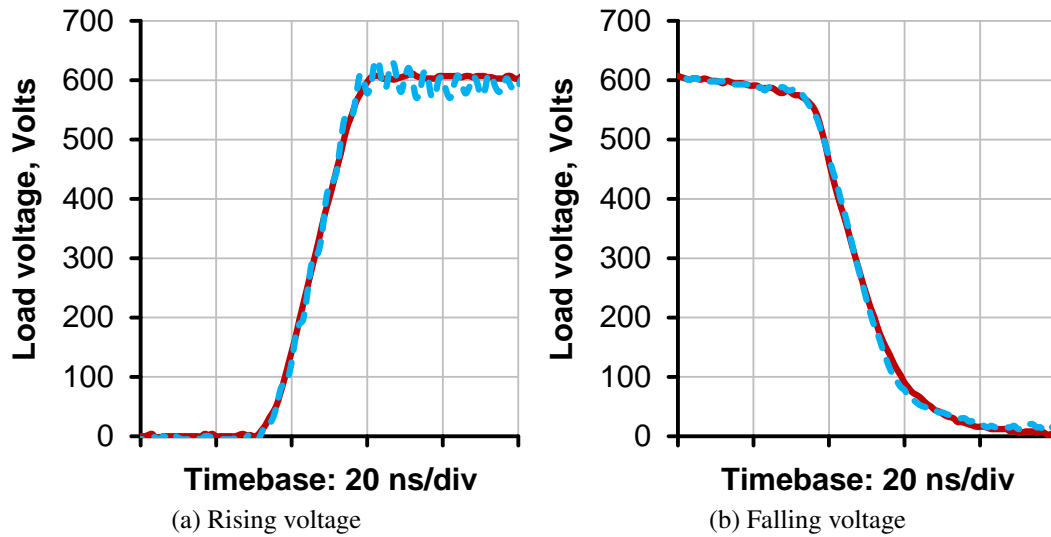


Figure 3.9: Resistive load voltage derived from voltage measurements (red solid line) and Rogowski current measurements de-skewed by +17.0 ns (blue dashed line)

Probe ID	Skew vs probe #1	Estimated precision
#1	0 (reference)	N/A
#2	-200 ps	± 20 ps
#3	+400 ps	± 20 ps
#4	-260 ps	± 20 ps
#5	+2.7 ns	± 100 ps
#6	+2.8 ns	± 100 ps
#7	+17.0 ns	± 500 ps

Table 3.3: Skew calibration of oscilloscope probes

3.7 Rogowski probe $\frac{dV}{dt}$ dependence

3.7.1 The need to measure drain current

Drain current (I_D) is the preferred terminal current measurement for power devices. This is because instantaneous power dissipation can be easily calculated from $I_D \cdot V_{DS}$ and doing so ensures that Miller currents are properly accounted for in switching loss measurements. It is also undesirable to measure current at the source of a transistor, since this unavoidably increases source inductance, which can significantly impair device switching performance.

3.7.2 Problems with drain current measurement

Measuring drain current with a Rogowski coil is complicated by the fact that the voltage at the drain can change rapidly. The resulting high $\frac{dV}{dt}$ experienced by the Rogowski coil can cause a displacement current to flow through its stray capacitance, resulting in an error voltage at its output that is directly proportional to $\frac{dV}{dt}$. The additional stray capacitance between the Rogowski coil and the PCB also reduces the damping factor of the Rogowski coil, making it more prone to parasitic oscillations [161].

One solution to this problem is to use a grounded electrostatic screen around the Rogowski coil. However, this reduces the bandwidth of the coil and must be implemented carefully; a screen forming a shorted coil around the probe would have a significantly detrimental effect on its high frequency performance [162].

3.7.3 Current correction in post-processing

An alternative method for correcting for Rogowski coil $\frac{dV}{dt}$ interference is to remove the noise by post-processing. To do this, it is necessary to know both $\frac{dV_{DS}}{dt}$ and I_D throughout the switching period and to know the constant that relates $\frac{dV_{DS}}{dt}$ to the measurement error.

This constant can be easily found if an accurate value for $I_{D(casc)}$ is known, as measured values can be compared against it. This is not possible to do directly with the Rogowski coil for the reasons already discussed. However, it can be calculated from measurements of $I_{S(casc)}$, $V_{G(HV)}$ and $V_{GS(LV)}$, all of which are unaffected by interference from $\frac{dV_{DS}}{dt}$:

$$I_{D(casc)} = I_{S(casc)} + \frac{V_{G(HV)} - V_{bias}}{R_{G(HV)}} + \frac{V_{drive}}{R_{gate(LV)}} \quad (3.3)$$

where V_{drive} is $V_{GH(LV)} - V_{GS(LV)}$ at turn-on and $V_{GS(LV)} - V_{GL(LV)}$ at turn-off and $R_{gate(LV)}$ is $R_{GH(LV)}$ at turn-on and $R_{GL(LV)}$ at turn-off.

3.7.3.1 Extracting Rogowski coil $\frac{dV}{dt}$ sensitivity

A circuit with a complex switching waveform was chosen to validate this technique. This was the SiC MOSFET/Si MOSFET cascode circuit of figure 6.14 in which a 100 pF capacitance was added between the HV drain and the LV gate to limit switching speed. It is discussed in detail in section 6.6.1.1. A feature of this circuit is the onset of instability, halfway through the switching transient, resulting in oscillatory transitions of $V_{DS(casc)}$ and $I_{D(casc)}$, especially at turn-off.

Measurements of $I_{D(casc)}$ and $I_{S(casc)}$ were taken for this arrangement using the Rogowski coil and $V_{G(HV)}$, $V_{GS(LV)}$ and $V_{DS(casc)}$ were also recorded. The actual value of $I_{D(casc)}$ during switching was then calculated by applying these measurements to equation 3.3. For accuracy, the gate driver resistance and device internal gate resistances were included in the values of $R_{G(LV)}$ and $R_{G(HV)}$. The effect of adding an additional current measuring loop at the cascode source to measure $I_{S(casc)}$ was small in this case, due to the comparatively large package inductance of the devices used.

The relationship between the Rogowski measurement error and $\frac{dV_{DS(casc)}}{dt}$ is shown in figure 3.10, for the rise and fall of $V_{DS(casc)}$ between 5 and 95 %. Measurements of $V_{DS(casc)}$ were smoothed before $\frac{dV_{DS(casc)}}{dt}$ is calculated to avoid introducing excessive noise into the measurements. This was done using exponential smoothing with a time constant of 5 ns, to give a measurement bandwidth equivalent to that of the Rogowski coil. By only considering the relationship between Rogowski measurement error and $\frac{dV_{DS(casc)}}{dt}$ whilst $V_{DS(casc)}$ is changing, the confounding effects of parasitic oscillations in the Rogowski coil are removed.

Figure 3.10 shows a strong, linear correlation between the error in Rogowski coil measurements of $I_{D(casc)}$ and $\frac{dV_{DS(casc)}}{dt}$. The Rogowski coil appears to be slightly more strongly affected by negative $\frac{dV_{DS(casc)}}{dt}$ (0.79 A s GV^{-1}) than by positive $\frac{dV_{DS(casc)}}{dt}$ (0.62 A s GV^{-1}), which may be due to non-linear capacitive coupling behaviour. Nevertheless, this strong correlation indicates that current measurement error due to $\frac{dV}{dt}$ interference should be easily removed by post-processing current measurements.

3.7.3.2 Method validation

The measured, actual and corrected values of $I_{D(casc)}$ for a set of switching transients from the validation test circuit are compared in figure 3.11. It is very clear from this figure that direct Rogowski measurements of $I_{D(casc)}$ (green dashed line) bear little relation to the actual value of $I_{D(casc)}$ (dashed light blue line), as a result of $\frac{dV}{dt}$ interference. Direct Rogowski measurements of $I_{D(casc)}$ are therefore clearly unsuitable for this experimental work.

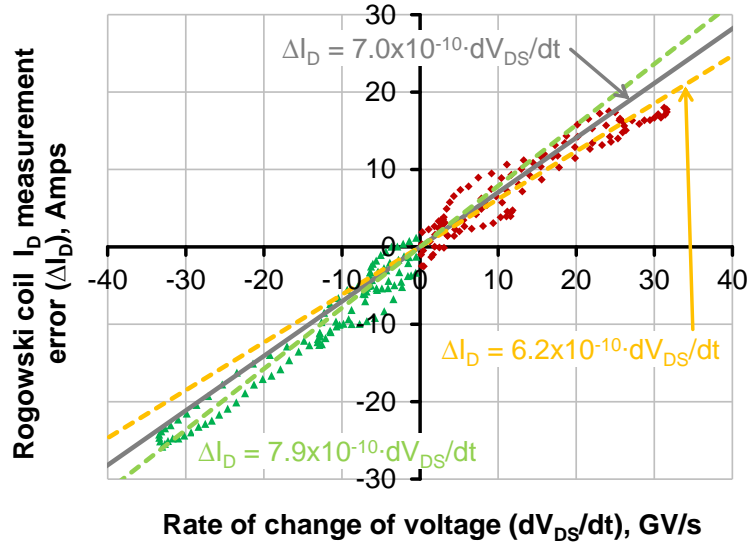


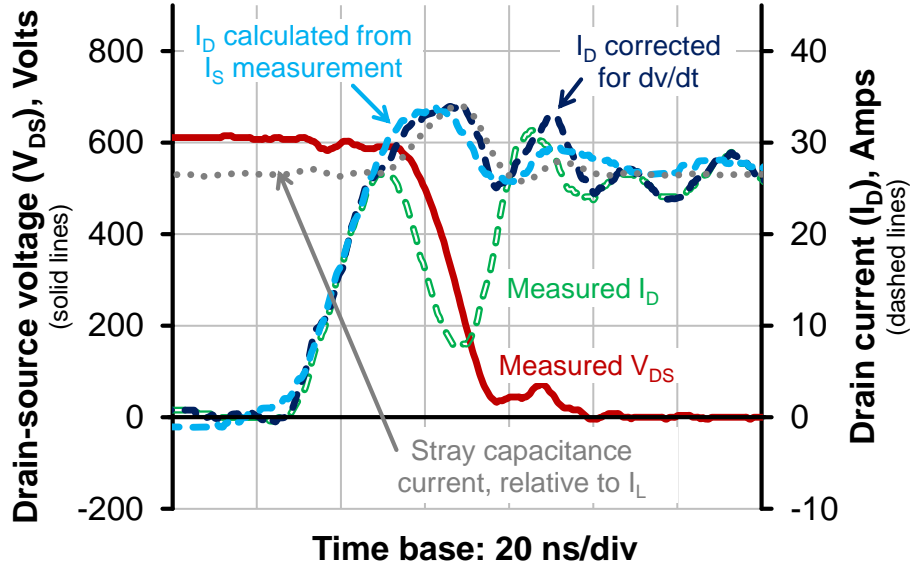
Figure 3.10: Relationship between $\frac{dV_{DS(casc)}}{dt}$ and Rogowski coil I_D measurement error during cascode voltage rise and fall.. The solid grey line of best fit is for all the data, whilst the dashed orange and light green lines show the best fit for positive and negative values of $\frac{dV_{DS(casc)}}{dt}$ respectively.

These measured values of $I_{D(casc)}$ were then post-processed to remove the effect of $\frac{dV_{DS(casc)}}{dt}$ using the sensitivities extracted in figure 3.10. This is represented as the dark blue dashed line in figure 3.11. These corrected data show a very good match with the calculated value of $I_{D(casc)}$ over the entire switching period, although they show slightly greater sensitivity to ringing. However, this does not significantly affect the calculation of parameters of interest such as rise and fall times or switching losses.

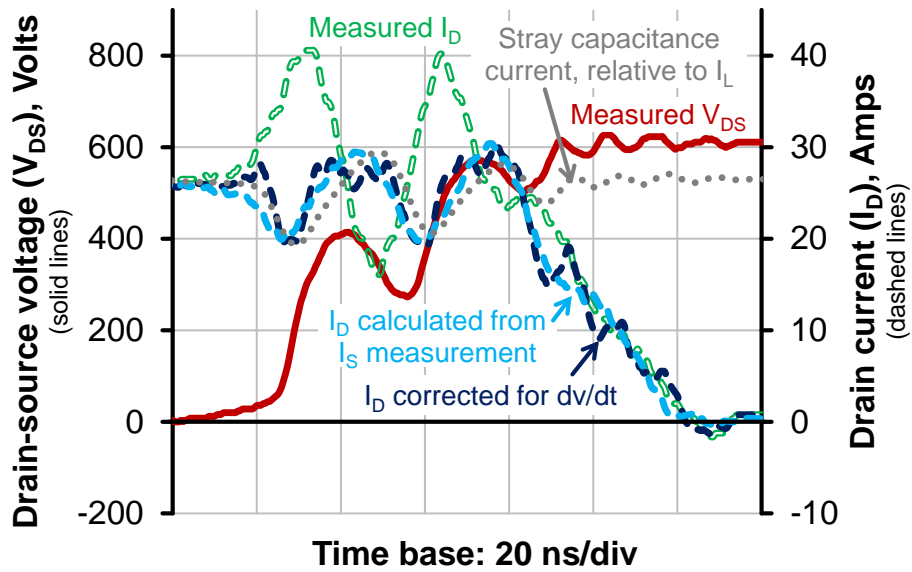
This shows that this method of correcting Rogowski measurements of $I_{D(casc)}$ in post-processing provides reasonable accuracy, whilst avoiding the disadvantages of measuring cascode source current.

3.7.3.3 Determining $\frac{dV}{dt}$ sensitivity

One complication remains: The sensitivity of the Rogowski coil to $\frac{dV}{dt}$ has so far been calculated using measurement of $I_{S(casc)}$. Although Rogowski coil position remains unchanged during each experiment, slight variations in coil position and therefore capacitive coupling between experiments mean that Rogowski coil $\frac{dV}{dt}$ sensitivity cannot be considered constant. It is therefore necessary to be able to calculate Rogowski coil $\frac{dV}{dt}$ sensitivity for each experiment, independently of measurements of $I_{S(casc)}$.



(a) Turn-on



(b) Turn-off

Figure 3.11: Switching waveforms comparing I_D measured with Rogowski coil with corrected I_D measurements, actual I_D measurement and $V_{DS(casc)}$. Measurements are taken for a cascode circuit consisting of a HV SiC MOSFET, LV Si MOSFET, $R_{GH(LV)} = 3.3 \, \Omega$, $R_{GL(LV)} = 3.3 \, \Omega$ and $R_{G(HV)} = 4.7 \, \Omega$ and a feedback capacitor of 100 pF in series with a 10 Ω damping resistor between the HV drain and LV gate (see section 6.6.1.1)

The capacitance between the cascode drain and small signal ground of the PCBs used in the experimental work has been measured as 172 pF. This appears in parallel with the junction capacitance of the free-wheel diode, which averages around 50 pF over the majority of the switching voltage range [155]. These capacitances are responsible for both the ‘reverse recovery’ current overshoot at turn-on as $V_{DS(casc)}$ falls and the initial fall in drain current as $V_{DS(casc)}$ rises, since the load current is otherwise held approximately constant by the inductive load. The parasitic capacitances of the MOSFETs do not contribute to these effects, due to the position of the Rogowski coil in the circuit.

This provides a convenient method for calculating the sensitivity of the Rogowski coil in a particular experiment. If the magnitude of the current over- or undershoot of the corrected $I_{D(casc)}$ waveform can be matched with that expected from the known capacitance between the cascode drain and small signal ground, then the sensitivity of the Rogowski coil to $\frac{dV_{DS(casc)}}{dt}$ is known.

This is shown to be an effective method in figure 3.11. The dotted grey line shows the expected variation in ‘apparent’ load current as a result of current flowing in the approximately 225 pF stray capacitance at the cascode drain as $V_{DS(casc)}$ changes, given that:

$$I_{L(apparent)} = I_L - C_{stray} \frac{dV_{DS(casc)}}{dt} \quad (3.4)$$

The magnitude of this expected variation matches closely with the variation in both the calculated value of $I_{D(casc)}$, as well as the ‘corrected’ value of $I_{D(casc)}$ determined by post-processing Rogowski coil $I_{D(casc)}$ measurements.

Since the post-processed $I_{D(casc)}$ measurements were calculated without reference to the effects of the PCB and free-wheel diode stray capacitance, this lends substantial confidence to the suitability of this technique.

3.8 PCB inductance characterisation

To properly quantify the effects of stray inductance on cascode switching, the inductance of the tracks on the test PCB must be characterised. This is particularly important in fast-switching circuits like the cascode where the frequency dependence of inductance can cause even small parasitic inductances to become significant.

The resistance of PCB tracks is not considered, since it is several orders of magnitude smaller than that of either the devices $R_{DS(ON)}$ or the gate resistances at frequencies into the GHz, even accounting for the skin effect.

3.8.1 Measuring small impedances

Measuring the impedance of PCB tracks is challenging. A typical trace has a complex impedance of a fraction of an ohm even at frequencies into the megahertz. Standard component analysers are not well suited to characterising such low impedances; typical maximum design frequencies are in the low MHz range and many implementations use only two-wire sensing.

To accurately measure small complex impedances, a more sophisticated RF technique, analogous to DC Kelvin (4-wire) sensing, must be used. This is known as a 2-port measurement and is performed, using a Vector Network Analyser (VNA) [163]. A VNA has two ‘ports’, both capable of accurately synthesising and detecting sinusoidal voltage signals and is capable of precisely calculating the magnitude and phase of a detected signal relative to the synthesised signal.

3.8.2 VNA measurements

Either of the VNA ports may be used to provide the input or output, giving four possible ‘scattering parameter’ (S-parameter) measurements, known as S_{11} , S_{22} , S_{12} and S_{21} . In this notation, the first subscript represents the port where the output signal is measured, whilst the second subscript represents the port where the input signal is injected. Only S_{21} and S_{12} are two-port parameters suitable for measuring small impedances. For a passive network such as a PCB track, the effect of the network on a signal is not dependent on its direction of travel and hence $S_{21} = S_{12}$.

A VNA is an RF instrument and this must be considered in the implementation of the test circuit. Typically the VNA is designed for a 50 Ω system and test leads must be of the correct characteristic impedance to avoid unwanted reflections. Calibration is also necessary to remove the effects of parasitics that would otherwise corrupt measurements.

3.8.3 Measurement technique

The impedance of a PCB track is measured by connecting it in parallel with the port(s) of the VNA. The effect of the impedance of the PCB track (load) Z_L , on an RF signal applied across it from a transmission line of characteristic impedance Z_0 is described by the reflection coefficient equation:

$$\rho_L = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (3.5)$$

Z_L for a typical PCB trace can be approximated by a small resistance of the order of a few hundred microohms in series with a small inductance of the order of a few nanohenries. At low

frequencies, this ensures almost perfect reflection of an injected signal. Hence $S_{11} = S_{22} \approx 1$ and $S_{12} = S_{21} \approx 0$. Even at higher frequencies, ρ_L is likely to be close to 1. For example, even a PCB track with 10 nH of inductance will only match the magnitude of Z_0 at a frequency of around 800 MHz.

If reflection measurements (S_{11} and S_{22}) are used to measure Z_L , the reflection coefficient will be close to 1, making it difficult to accurately determine the inductance of Z_L , since the difference in response between Z_L and a dead short will be extremely small. Additionally, variations in lead impedance arising from the PCB probe connections will be indistinguishable from the impedance of Z_L using this method.

In contrast, two-port transmission measurements (S_{21} and S_{12}) are capable of high accuracy when measuring a small Z_L . A VNA has a large dynamic range and is easily capable of detecting the transmitted signal. Furthermore, small variations in lead impedance cannot significantly influence the measurement.

3.8.4 VNA calibration

The VNA was calibrated using the SOLT (Short, Open, Load, Through) method. In a SOLT calibration, S_{11} and S_{22} are measured over the full range of test frequencies using a short circuit, open circuit and 50 Ω standard. S_{21} and S_{12} are then measured by connecting the test leads together.

Using these measurements, the VNA calculates an error matrix to remove the effects of stray inductance, capacitance and resistance in the test fixture. In effect, calibration relocates the plane of reference of the VNA from the front panel connectors to the end of the test leads, allowing accurate measurements to be taken.

3.8.5 Frequency limitations

For accurate measurements, the received signal must be well above the VNA noise floor. A smaller ρ_L and hence a higher measurement frequency is therefore preferable. However, there is a trade off with the practicality of making the measurements.

Due to the length and positioning of tracks on the test PCB, it is necessary to be able to measure impedance between points up to about 50 mm apart as well as between both sides of the PCB. As a result, test leads ('pigtailed') with a length of about 60 mm are required. Since these pigtailed cannot be of the system characteristic impedance, the maximum frequency for which the technique is valid is limited.

3.8.6 Calculation of inductance

For a 50 Ω VNA, the direct relationship between S_{21} and Z_{DUT} may be shown to be [163]:

$$Z_{DUT} = \frac{S_{21}}{1 - S_{21}} \cdot 25 \Omega \quad (3.6)$$

This is adequate when only the magnitude of the impedance is of interest, but further information is required to calculate its inductive and resistive components. To do this, S_{21} must be expanded into its real and imaginary parts (i.e. $S_{21} = a + bj$), by extracting these data separately from the VNA. Substituting into equation 3.6 relating Z_{DUT} to S_{21} gives:

$$Z_{DUT} = \frac{a(1 - a) - b^2 + bj}{(1 - a)^2 + b^2} \cdot 25 \Omega \quad (3.7)$$

Where $a = \Re(S_{21})$ and $b = \Im(S_{21})$

By taking the real and imaginary parts of this expression, precise relationships for the PCB track resistance and inductance may be derived, assuming it behaves as a simple series R-L circuit.:

$$R_{DUT} = \Re(Z_{DUT}) = \frac{a(1 - a) - b^2}{(1 - a)^2 + b^2} \cdot 25 \quad (3.8)$$

$$L_{DUT} = \Im(Z_{DUT}) = \frac{bj}{(1 - a)^2 + b^2} \cdot \frac{25}{\omega} \quad (3.9)$$

These equations are applied to the raw data from the VNA to calculate resistance and inductance over the full frequency range. Figure 3.12 shows typical measurements of inductance from the power tracks of the test PCB over a wide frequency range.

The graph clearly shows an arbitrary inductance measured at low frequency due to insufficient signal to noise ratio, a relatively flat inductance at intermediate frequencies and arbitrary inductance at higher frequencies as transmission line reflections become significant. The slight decrease in inductance as frequency increases over the intermediate frequency range is likely to be due to a small amount of parasitic capacitance in the test leads.

3.8.7 Test set-up

An Agilent 300 kHz - 3 GHz E5062A VNA was used to characterise PCB inductance. Before measurements were taken, the instrument was allowed to warm up for 10 minutes to avoid measurement drift. A logarithmic frequency sweep from 1 MHz to 100 MHz was used with at least 400 points, to provide sufficient resolution to detect anomalies in the traces. The dynamic range was enhanced by setting the intermediate frequency (IF) at 1 kHz and averaging

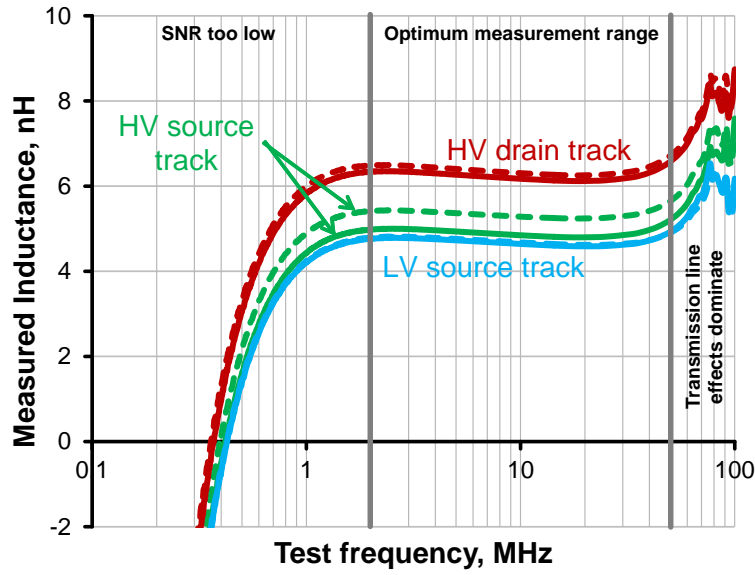


Figure 3.12: Inductance measurements for three PCB power tracks, for both upper switch (dashed lines) and lower switch (solid lines) over a wide frequency range.

measurements over at least 3 readings, to give an estimated minimum of 100 dB of dynamic range.

Separate measurements of real and imaginary S_{21} were taken using the VNA and post-processed to accurately calculate inductance over a wide frequency range. Each inductance measurement was graphed to ensure approximately constant inductance had been measured as expected over the frequency range of interest. The magnitude of each inductance measured at 10 MHz was then used as the representative value for that set of measurements, since this gives a value approximately in the middle of the region of constant inductance.

3.8.8 PCB measurement assumptions

It was not practical to directly measure the inductance of the circuit with the transistor dies in place, due to the need to encapsulate them for protection. Inductance measurements were therefore made on an unpopulated PCB, with component packages substituted with copper tape soldered between the component pads.

Although this does not perfectly replicate the populated PCB, errors due to this approach should be small. For instance, the JFET die described in section 3.2.2 with dimensions of 2.5 x 2.2 x 0.27 mm can be estimated from equation 3.2 to have an inductance of 0.06 nH [152]. Similarly, the inductance of bond wires has already been shown to be negligible in section 3.2.2.1.

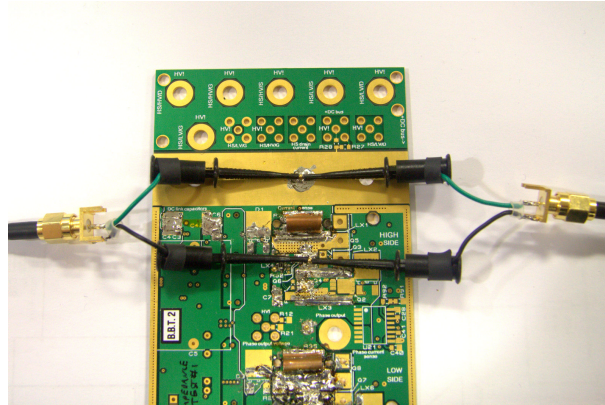


Figure 3.13: Connection of pigtailed test points to measure PCB track inductance

3.8.9 Test connections

For practicality and repeatability, low profile surface mount test points were soldered at both ends of PCB tracks of interest. The test pigtailed were manufactured with two leads from a subminiature version A (SMA) socket terminating in a spring-loaded SMD grabber to enable simple connection to the PCB test points as shown in figure 3.13. The total length of each pigtail was approximately 60 mm and the length was not affected by the spring-loaded action of the grabber. Given the low maximum frequency and two-port measurement technique used, this method was able to provide repeatable measurements even with minor variations in the position of the pigtail connections.

The pigtail connections form inductive loops with an inductance that depends on their precise geometric arrangement. This has a negligible effect on impedance measurements, provided the change in inductance is small compared to the 50 ohm input and output impedances. However, the input and output pigtailed must not be linked inductively to avoid errors due to cross talk. Connections to the PCB track were therefore made orthogonally to it [164] and test leads were connected at 180° to each other to minimise their mutual inductance.

3.8.10 PCB analysis and measurements

To simplify the analysis of the PCB trace inductance, the PCB was split into several sections as shown in figure 3.14 and table 3.4.

Measurements of self inductance for each of these tracks are shown in table 3.5. The readings are reasonably consistent, with less than 1 nH difference between the measurements for similar positions between the upper and lower switches. The self inductances measured are low and of the order expected given the dimensions of the conductors.

Location name	PCB trace location
A	Upper HV drain to +VDC bus
B	Upper HV source to upper LV drain
C	Upper LV source to half-bridge centre point
D	Lower HV drain to half-bridge centre point
E	Lower HV source to lower LV drain
F	Lower LV source to 0V bus
G	Upper HV gate input connection
H	Upper HV gate decoupling capacitor
I	Lower HV gate input connection
J	Lower HV gate decoupling capacitor
K	Upper LV gate input connection
L	Upper LV gate drive source reference
M	Lower LV gate input connection
N	Lower LV gate drive source reference

Table 3.4: Details of PCB inductance measurement sections

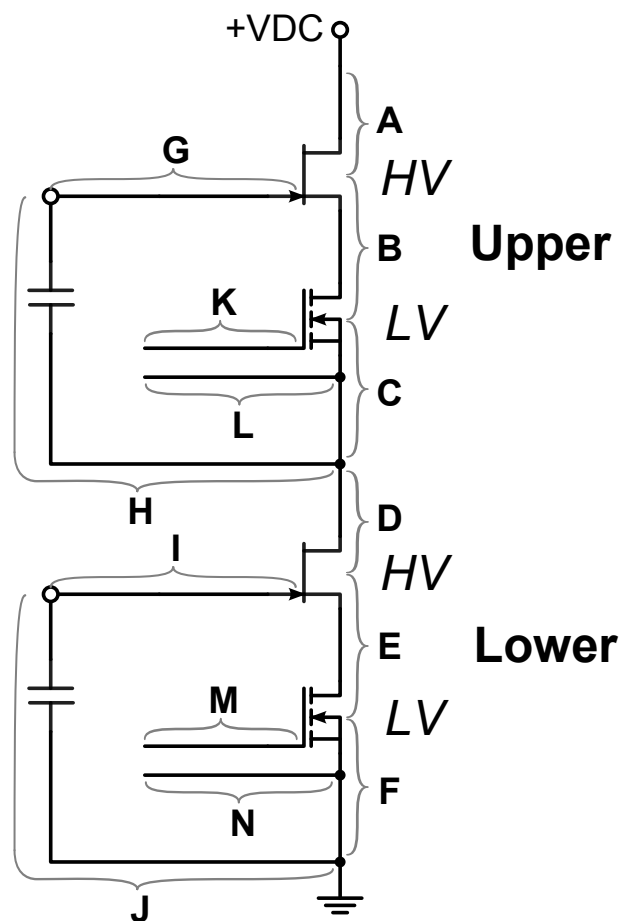


Figure 3.14: PCB inductance measurement sections

Upper		Lower	
Position	Self inductance	Position	Self inductance
A	6.4	D	6.6
B	5.3	E	4.8
C	4.7	F	4.6
G	6.9	I	5.9
H	5.8	J	5.0
K	6.9	M	6.9
L	8.2	N	8.4

Table 3.5: Measured PCB inductances for upper and lower switches (nH). Measurements on the same line are for tracks with similar PCB layout.

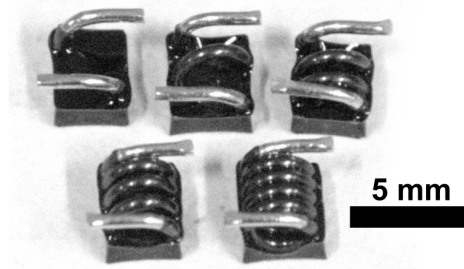


Figure 3.15: Coilcraft mini-spring coil inductors, showing 1 - 5 turn variants

3.8.11 Additional inductances

To measure the effect of inductances on the switching behaviour of the circuit, it is necessary to be able to repeatably add known inductances to the circuit in various locations. A set of surface mount Coilcraft air-core ‘mini-spring’ inductors with a tolerance of 5% were used for this purpose and the change in inductance of the tracks to which they had been added was measured using the same method as before (figure 3.15).

The orientation of the coils produces a magnetic field orthogonal to that of the PCB tracks, so the additional inductance due to the coils can be assumed to be approximately independent of the PCB track inductance.

3.8.12 Analysis of errors

The accuracy and repeatability of adding additional inductance to the PCB was investigated by comparing the theoretical and measured increase in PCB track inductance measured when mini-spring inductors of various sizes were added to the PCB. The relationship between the measured increase in inductance and the nominal additional inductance is shown in figure

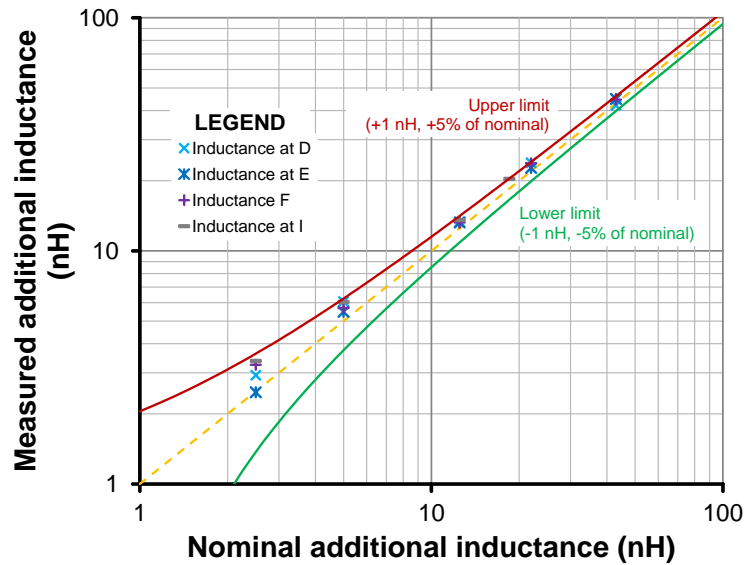


Figure 3.16: Measured vs. nominal additional inductance for 20 inductance measurements. Solid lines show expected upper and lower limits given a total error of ± 1 nH, $\pm 5\%$.

3.16. These measurements are tightly distributed, but with a greater percentage variation at small nominal inductances.

This implies that there is both an absolute and relative component to the accuracy of the result. By estimation from figure 3.16, it appears that the absolute measurement error is of the order of ± 1 nH and that absolute error is within the tolerance of the inductors used at $\pm 5\%$.

Care must be therefore be taken when interpreting the measured value of small inductances, since the absolute measurement error becomes large compared to the actual inductance. Figure 3.16 suggests that the measurement technique slightly over-estimates inductance, with almost all measurements of additional inductance being slightly higher than nominal.

Nevertheless, these measurements suggest that the effect of adding inductance at any location in the circuit is repeatable, within the error margins described. This is particularly useful for experiments where it is impractical to measure the actual inductance of the test PCB *in situ*.

3.9 Summary

The experimental techniques presented in this chapter show the consideration that has been given to ensure the reliability of results.

By minimising sources of measurement error and quantifying remaining errors, the experimental measurements of following chapters can be interpreted confidently and their limitations easily understood.

Chapter 4

Modelling a wide bandgap cascode switch

4.1 Introduction

Circuit modelling is an important tool for investigating complex circuit behaviour, without the limitations of experimental measurements. A good WBG cascode model is particularly helpful in this work, as a way of expanding the scope of the work to include measurements that would not otherwise be experimentally practicable; for example, by greatly increasing the resolution of measurement points, or by allowing measurement of parameters that are inaccessible with test equipment. To ensure confidence in a circuit model, its predictions must be validated against experimental measurements and its limitations properly understood.

In this chapter, SPICE modelling is introduced and its suitability for modelling cascode circuits is discussed. A SPICE model of a Semisouth SiC JFET is developed and incorporated into a simulated clamped-inductive cascode switching circuit. A simplified and linearised mathematical description of cascode hard-switching is then derived to describe the dominant parameters influencing the switching process. Both the SPICE model and the linearised model of cascode switching are validated by comparison with experimental measurements.

4.2 SPICE simulation

4.2.1 Origins

SPICE originated from the work of Nagel and Pederson [165] at the University of California, Berkeley in 1972. They aimed to develop a general-purpose simulation tool for the increasingly complex integrated circuits (ICs) that were becoming available at the time. SPICE uses nodal analysis to calculate the behaviour of circuits and has been capable of performing direct current (DC), alternating current (AC) and transient analyses from the earliest versions.

SPICE has been under continual development since its inception and the sophistication and range of available models and analyses has increased over time [166, 167]. However, SPICE remains a fundamentally command-line driven program, relying on text-based netlists to describe circuits. To improve its accessibility, a number of commercial organisations have developed user interfaces for SPICE, which include schematic capture and graphical output.

SPICE is an attractive choice of simulation tool, since it is a non-linear circuit simulator. This makes it particularly appropriate for modelling switching transients of transistors, in which device behaviour is by definition non-linear.

4.2.2 LTSpice

The LTSpice IV SPICE simulator from Linear Technology is used in this work. This is a well-regarded [168] freely-available circuit simulator based on the latest versions of SPICE (3F4/5). Linear Technology promote the simulator to market their own products and so it is optimised specifically for switch-mode applications [169]. In addition to the SPICE engine at its core, it benefits from a graphical schematic capture tool, graphical waveform output, and sophisticated mathematical and measurement capabilities.

4.3 Modelling approach

The SPICE models developed here are used to inform the following experimental work. Similar devices and test set-ups to those used in the following experimental chapters are therefore simulated:

4.3.1 Device selection

4.3.1.1 HV SiC JFET

A Semisouth SJDP120R085 SiC normally-on JFET was chosen as the HV switch for the SPICE model. This is a useful device to model since, as a depletion-mode transistor, it benefits directly from the enhancement-mode behaviour of the cascode circuit. It was also available as a bare die, making it a possible to minimise its packaging inductance. This is an important consideration when investigating the effects of stray inductance on cascode switching (section 6.5).

As well as having specific advantages for circuit protection applications [76], the behaviour of a SiC JFET cascode can be easily related to cascodes based on other WBG devices such as SiC MOSFETs and GaN HEMTs; the comparable magnitude of circuit parasitics and device

ratings for these different device types makes direct circuit-level comparison reasonable, even if their carrier-level behaviour is somewhat different.

4.3.1.2 LV FETs

Two LV devices were investigated for use in a cascode circuit:

EPC2015 eGaN FET The enhancement-mode EPC2015 40 V, 33 A GaN field-effect transistor (FET) from the Efficient Power Conversion Corporation (EPC) allows the creation of an entirely WBG cascode switch. Whilst the EPC2015 benefits from a high transconductance and a very low on-state resistance of 3 m Ω , it suffers from an exceptionally delicate gate ($|\hat{V}_{GS}| = 6$ V) and a very low threshold voltage of approximately 0.7 V [170]. Great care must therefore be taken with its gate drive to avoid it exceeding its rating or experiencing spurious turn-on.

This device is mostly of interest to examine the possible advantages of an entirely WBG cascode. Additionally, its extremely low inductance bumped die package makes it useful for investigating the effects of stray inductance in section 6.5.

Fairchild FDMS5352 The Fairchild FDMS5352 is a 60 V, 49 A trench MOSFET [171]. It is representative of a conventional LV silicon transistor that might be used in a commercial application. It is packaged in a low inductance PQFN surface mount package and has typical logic-level gate drive requirements. This device is used in experimental work in chapters 5 and 6, comparing cascodes based on different HV devices.

4.3.2 Clamped inductive load

The clamped inductive load, described in section 3.5 and used in later experimental work, is replicated in the cascode SPICE model. This allows the model to both be validated directly from experimental measurements and also to complement and extend experimental measurements.

4.4 SiC JFET Modelling

4.4.1 Manufacturer's model

A model of the Semisouth SiC JFET created by the manufacturer is an obvious starting point for a SPICE model of a SiC JFET cascode. It is listed fully in appendix A. This is a very simple model, derived from the Schichman-Hodges MOSFET equations and is similar to SiC

JFET models developed by other authors [172, 173]. It assumes a square law relationship between I_D and V_{DS} in the linear region and an essentially constant I_D with changing V_{DS} in the saturation region given by [166]:

$$I_D = \begin{cases} 0 & V_{GS} - V_T < 0 \\ \beta(V_{GS} - V_T)^2(1 + \lambda V_{DS}) & 0 < V_{GS} - V_T < V_{DS} \\ \beta V_{DS}[2(V_{GS} - V_T) - V_{DS}](1 + \lambda V_{DS}) & 0 < V_{DS} < V_{GS} - V_T \end{cases} \quad (4.1)$$

Where β is the forward transconductance parameter and λ is the channel-length modulation parameter.

The voltage-dependent gate-source and drain-gate capacitances in the JFET model are described by an inverse square-law relationship, whilst the intrinsic gate-source and gate-drain P-N junction diodes are modelled using the idealised Shockley diode equation. The inclusion of λ in the model is a rudimentary approach to model short-channel effects in the JFET.

4.4.2 Validation of Semisouth SiC JFET model

The SiC JFET SPICE model's simulated I-V characteristics are compared with those from curve tracer measurements of the JFET in figure 4.1. It is immediately apparent that there is a poor match between simulation and experiment, particularly in the saturation region, where the model predicts approximately constant I_D with increasing V_{GS} , which is not observed in the measurements.

4.4.3 High-power I-V measurements

4.4.3.1 Self-heating

Although figure 4.1 indicates problems with the manufacturer's model, it does not describe how the JFET behaves at higher V_{DS} , nor how effective the model is at representing it. This is particularly important when considering clamped inductive switching, where the device operates far into its saturation region for almost the entire hard-switching process.

Experimental measurements in the saturation region are complicated by the susceptibility of the device to self-heating (see section 5.5). As a result of its high current rating, the instantaneous power dissipated in the channel of the JFET when operating in its saturation region may easily exceed 1 kW, even at a V_{DS} of a few tens of volts. The pulse width of a conventional curve tracer is sufficiently long to cause significant self-heating of the channel during the measurement period under these conditions. This effect cannot be solved by heat-sinking;

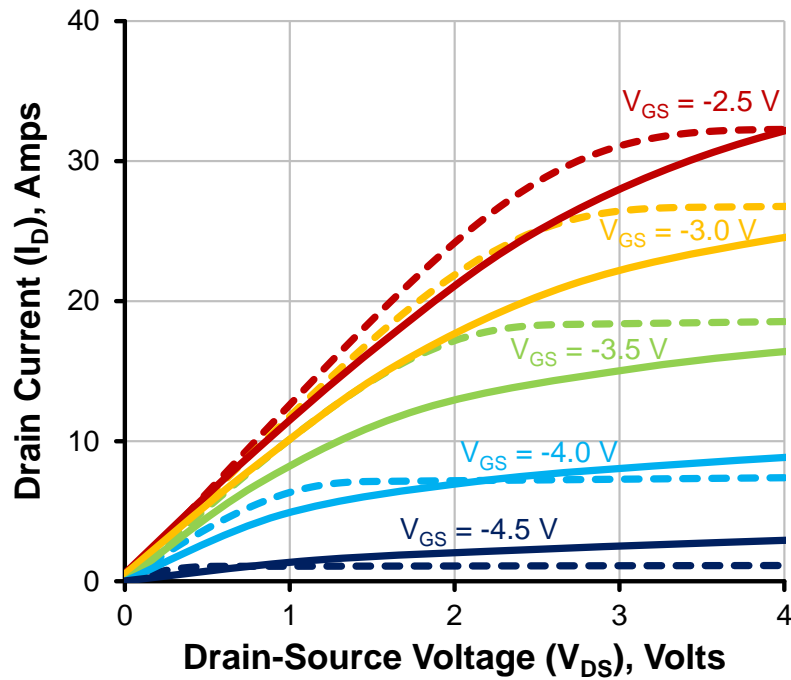


Figure 4.1: Comparison between simulated and measured JFET I-V characteristics. Solid lines are experimentally measured values and dashed lines are SPICE simulations using Semi-south's model

the channel temperature rises very rapidly locally before heat can be conducted through the substrate.

4.4.3.2 Short pulse-width measurements

To avoid this problem, a custom short pulse-width curve-tracing set-up was constructed, as described in section 3.5.2. The short pulse-width of this technique makes it possible to measure I-V curves for the JFET up to a V_{DS} of 30 V with negligible self-heating. The JFET I-V characteristics measured using this set-up are compared to those made with a Tektronix 371A curve tracer in figure 4.2. There is an excellent match between the traces in the linear region, but the measurements diverge due to self-heating of the device in the conventional curve tracer as I_D and V_{DS} increase.

Unsurprisingly, the divergence is proportional to power dissipation and becomes significant above an instantaneous power of 200 W. This power level is represented by a dotted grey line in figure 4.2 and represents the limit for accurate measurement of JFET characteristics using the conventional curve tracer. In contrast, the short pulse-width technique can be estimated to be accurate up to an instantaneous power of around 9 kW, based on linearly scaling the

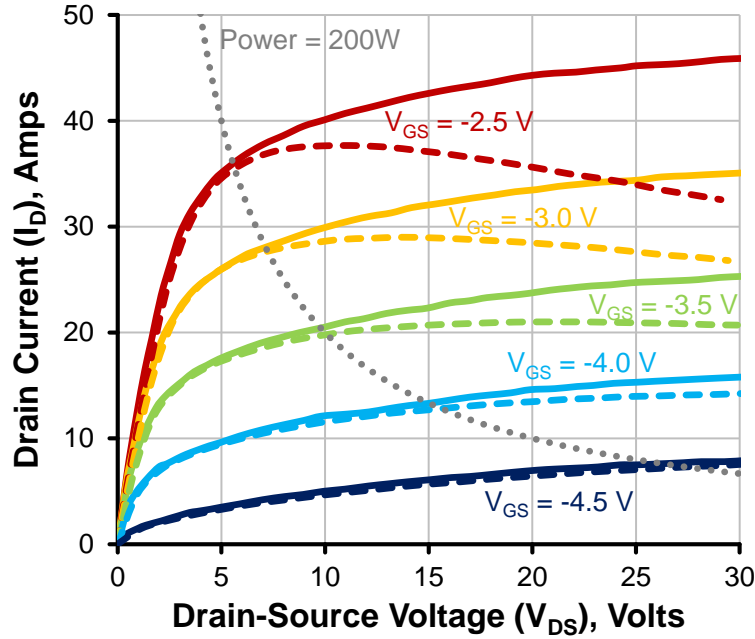


Figure 4.2: I-V curve for Semisouth SJDP120R085 SiC JFET using short pulse-width measurement technique (solid lines) vs. Tektronix 371A curve tracer measurements (dashed lines). A power dissipation of 200 W is represented by the dotted grey line

ratio of the pulse widths. In this implementation however, V_{DS} may not exceed 30 V, due to the voltage rating of the drain-source capacitor bank.

4.4.3.3 Comparison with Semisouth model

I-V curves for the SiC JFET from the short pulse-width experimental measurements are compared with those predicted by the Semisouth model in figure 4.3. Whilst the model bears some relation to JFET's behaviour in the linear region, it is entirely inadequate at describing its behaviour in the saturation region. In particular, it fails to model both the very smooth transition between linear and saturation region and the continuing rise of I_D with V_{DS} throughout the saturation region.

Not only is this evidence of poor modelling by the manufacturer, but it also shows that the Schichman-Hodges equations on which the model is based are fundamentally too simplistic to accurately describe the JFET's saturation region. An alternative model of the JFET is therefore required, for which it is first necessary to properly understand its behaviour in the saturation region.

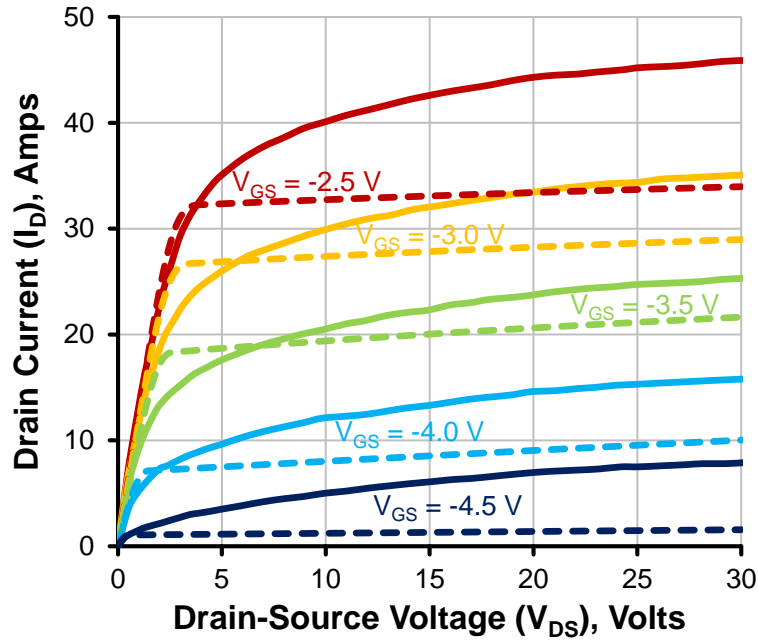


Figure 4.3: I-V curve for Semisouth SJDP120R085 SiC JFET using short pulse-width measurement technique (solid lines) vs. Semisouth SPICE model simulations (dashed lines).

4.4.4 Short channel effects

The discrepancy between the experimental measurements and the manufacturers SPICE model can partly be explained by the presence of short channel effects, specifically those of velocity saturation and channel length modulation. These come about due to the short length of the JFET channel relative to its width and the significant voltages it is required to block. As a result, high electric fields exist within the device during operation, and its behaviour departs from that of the Schichman-Hodges model.

4.4.4.1 Velocity saturation

Mobility is an important design parameter for FETs. When a low-level electric field is applied to a semiconductor, there is a linear relationship between carrier velocity and electric field such that:

$$v(E) = \mu_0 E \quad (4.2)$$

Where μ_0 is the mobility under low field conditions.

A higher mobility allows charge carriers to travel faster for a given applied electric field, resulting in a greater current for a given applied voltage. High mobility is therefore desirable in a power transistor to increase current ratings and to maximise power density. Under low

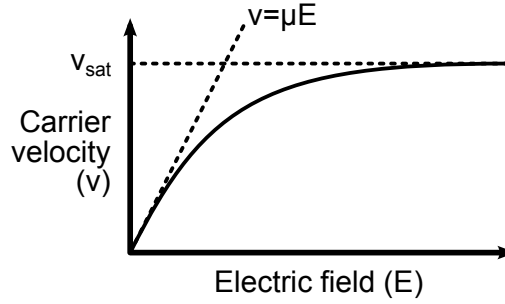


Figure 4.4: Effect of electric field on carrier velocity

field conditions, Si has a mobility about double that of SiC [37], which explains why Si is preferred for low voltage, high current devices.

This linear relationship between carrier velocity and electric field breaks down at higher field strengths. As the velocity and hence the energy of the carriers increases, it becomes possible for them to lose energy by emitting an optical phonon [174]. This becomes significantly more likely as field strength and hence carrier energy rises. The overall effect of this process is to cause the average carrier velocity to saturate and tend asymptotically to a limiting value v_{max} (figure 4.4).

Consequently, the relationship between V_{GS} and I_D becomes approximately linear, rather than quadratic, leading to substantially lower I_D for a given V_{GS} than might otherwise be expected. Velocity saturation is not accounted for in the Schichman-Hodges model.

4.4.4.2 Channel length modulation

Channel length modulation occurs when the influence of the electric field associated with the drain voltage causes the effective channel length under the control of the gate to decrease as drain voltage rises. A shorter effective channel length leads to a lower channel resistance, with the result that I_D continues to rise as V_{DS} increases throughout the saturation region.

Although a channel length modulation parameter (λ) is included in the Schichman-Hodges model, it is assumed to be a constant. However, as is obvious from figures 4.2 and 4.3, λ must itself be dependent on V_{DS} , since the rate of increase of I_D with V_{DS} clearly falls with increasing V_{DS} .

4.4.5 Development of an improved model

The development of an improved SPICE model for the SiC JFET is hampered by poor modelling support for power JFET devices. The simplistic Schichman-Hodges JFET model is the only native SPICE JFET device and is itself based on the Shockley JFET equivalent cir-

cuit [175], which is commonly used to model JFETs as SPICE sub-circuits. Neither of these approaches adequately accounts for the short channel effects that have been encountered.

4.4.5.1 Other approaches

Some authors choose to ignore this problem completely and treat SiC power JFETs as signal-level devices by using the native SPICE JFET model and improving the parameter extraction process [172, 173]. Naturally, these authors claim a good fit with experiment, but typically only attempt to fit their models over a limited voltage range, for which short channel effects are insignificant. Whilst these limitations are at least acknowledged by some authors [173], this approach is clearly inappropriate here.

More sophisticated modelling of SiC vertical JFETs has been undertaken by Platania and Chen [64, 176] who formulated detailed mathematical descriptions of device behaviour based on models of the fundamental device physics, including the effects of field-dependent mobility. However, although channel-length modulation can also be included in both models, it is only considered as a linear term, which limits their accuracy in the saturation region.

The fundamental nature of these models also requires a complete picture of all device parameters, including geometry and doping concentrations. This was not available for the JFET used, due to a lack of information from the manufacturer. Furthermore, the complexity of Chen's model makes it challenging to implement as a compact model in a SPICE environment.

An alternative approach for modelling the SiC JFET is therefore required, which is more sophisticated than the native SPICE JFET model, but that does not rely on unknown manufacturing parameters. A semi-empirical MOSFET SPICE model is one such solution.

4.4.5.2 MOSFET SPICE models

The continual reduction in transistor feature size has long since made the modelling of short-channel effects in IC MOSFETs a necessity. Consequently, a large number of sophisticated SPICE MOSFET models have been developed to account for the many non-idealities of modern MOSFETs. Hence, if the behaviour of the SiC power JFET can be related to that of a silicon MOSFET, it may be possible to use an existing model to describe its operation.

This approach presents two challenges: A lack of information about the JFET geometry and semiconductor properties means that several parameters will need to be found by estimation and tuning of the model. Secondly, most MOSFET models are intended to model lateral devices, rather than vertical devices such as the JFET. Whilst a lateral device model can feasibly describe the short-channel behaviour of the JFET, it is unrealistic to expect it to also

accurately describe the behaviour of device capacitances. In contrast, one of the few models specifically intended to simulate vertical devices has a sophisticated capacitance model, but does not account for short channel effects. For this reason, a hybrid approach is required.

4.4.5.3 A hybrid model

Three aspects of JFET behaviour must be accurately captured in an effective model: Its I-V characteristics, the behaviour of its non-linear parasitic capacitances and the effect of its gate-source and gate-drain diodes. Since it is not feasible to accurately capture these aspects of JFET operation with a single MOSFET model, they will instead be modelled independently using individual SPICE models and combined into a subcircuit to create a hybrid SPICE model of the SiC JFET:

- The JFET I-V characteristics will be described using the lateral level 3 MOSFET model to ensure its short channel behaviour is accounted for.
- Devices capacitances will be modelled using the VDMOS MOSFET model, since this is specifically intended to simulate vertical device capacitance.
- As the JFET is the only type of FET with intrinsic gate diodes, this behaviour is not described by any MOSFET model. The gate junctions are therefore modelled as discrete components in the hybrid circuit.

4.4.6 Level 3 MOSFET model

The SPICE level 3 MOSFET model (MOS3) is intended as a “semi-empirical model for small-geometry MOSFETs” [177] This makes it particularly suitable for modelling the characteristics of the JFET. As an early small-geometry lateral MOSFET model, released in 1975 [166], it accounts for short-channel effects without the complexity of recent models, which often require detailed knowledge of device processing parameters. Many of the level 3 parameters can also be determined by simple static device measurements such as transfer and I-V characteristics. It also makes use of several empirical parameters to aid fitting the model to experimental measurements. A full explanation of the parameters discussed below is given by Vladimirescu and Liu [177].

4.4.6.1 Neglected parameters

Several modifications must be made before the MOS3 model can be made to be applicable to the vertical JFET and a number of parameters are either irrelevant or must be disabled as follows:

Capacitances Being intended for lateral devices, the MOS3 capacitance model is not applicable to the vertical JFET and are instead included separately using the VDMOS model. All capacitance parameters in the MOS3 model are therefore either set to zero, or become irrelevant, thus avoiding interference with those of the VDMOS model. This includes the parameters CBD, CBS, CGSO, CGDO, CGBO, CJ, CJSW, FC, MJ, MJSW and PB.

Body diode There is no intrinsic body diode in the JFET structure, but the MOS3 model assumes one exists. To disable this part of the model, the diode saturation current IS is set to zero. This also makes the parameters N and JS irrelevant to the model.

Noise Noise analysis is not relevant to the modelling of device switching, hence noise parameters KF and AF are neglected.

Temperature Although temperature can be important in modelling power devices, it is not included as part of this SPICE model as it is not necessary for understanding cascode switching behaviour. The nominal temperature TNOM therefore defaults to 27 °C.

Device dimensions A series of parameters exist to scale irrelevant device parasitic capacitances and resistances based on device geometry. Since these either default to zero or are overridden by other parameters, AD, AS, PD, PS, NRD, NRS and RSH are ignored.

Threshold parameters The MOS3 model is able to calculate threshold voltage and calculate sub-threshold currents. Since the threshold voltage can easily be measured and the device is controlled by pinch-off rather than an inversion layer, the parameters NSS and NFS are neglected. Additionally, the TPG parameter is set to 0, to simulate an Aluminium rather than polysilicon gate.

4.4.6.2 Extraction of key parameters

For a SPICE model to be representative of the component it is simulating, the values of different model parameters must be extracted from the known behaviour of the device as follows:

Electrical parameters Electrical model parameters can be extracted from the static characteristics of the JFET.

The threshold voltage (VTO), intrinsic transconductance (KP) and source resistance (RS) can all be calculated from a plot of $\sqrt{I_D}$ against V_{GS} (figure 4.5). In the saturation region, the drain current is approximately related to V_{GS} by:

$$I_D = \frac{W}{2L} \cdot KP \cdot (V_{GS} - V_T)^2 \quad (4.3)$$

Hence by taking the square root of this relationship, KP can be found directly as:

$$KP = 2 \frac{L}{W} \times \text{gradient}^2 = 12.7 \frac{L}{W} \quad (4.4)$$

where L and W are determined by the geometry of the transistor. Following the determination of L and W, described later, KP is found to be 18.6.

If a straight line is extrapolated from the initial slope of this graph, its intercept with the V_{GS} axis is the threshold voltage, VTO. In this case, VTO = -5.24 V.

RS may be estimated using the deviation of the experimental measurements from the initial slope of the plot in figure 4.5. This deviation includes both the effect of the source resistance and that of velocity saturation. RS is therefore best estimated by finding the deviation between the two curves at a comparatively low V_{GS} and treating the value as an upper bound. In this case, RS was estimated using the deviation at $\sqrt{I_D} = 7 \text{ A}^{\frac{1}{2}}$ to give:

$$RS \approx \frac{\Delta V_{GS}}{I_D} \approx 15 \text{ m}\Omega \quad (4.5)$$

The drift region resistance RD is also calculated from static measurements. Since the initial slope of the I-V curve at full enhancement is limited only by the source and drain resistances, the initial gradient of the JFET I-V curve (see section 5.3.1) for $V_{GS} = 2.5 \text{ V}$ is approximately the sum of RS and RD. In this case, the gradient was measured as 64 m Ω , giving an RD of 49 m Ω . This value is somewhat higher than the source resistance since it includes the drift region resistance.

Geometric parameters To use a model intended for lateral MOSFETs to describe vertical JFETs, some parameters must be interpreted differently. The most obvious of these are the TOX and XJ which specify the MOSFET oxide layer thickness and metallurgical junction depth respectively. Neither of these parameters are directly relevant to the JFET, since it has no oxide layer and no P-N junction under the channel.

Without a P-N junction between the drain, source and substrate, XJ is meaningless and is therefore set to zero. TOX cannot simply be ignored however, since it describes the effect the gate charge has on the channel. Instead of an insulating oxide layer, the JFET has a depletion region between the channel and gate. TOX is therefore used to describe this depletion region

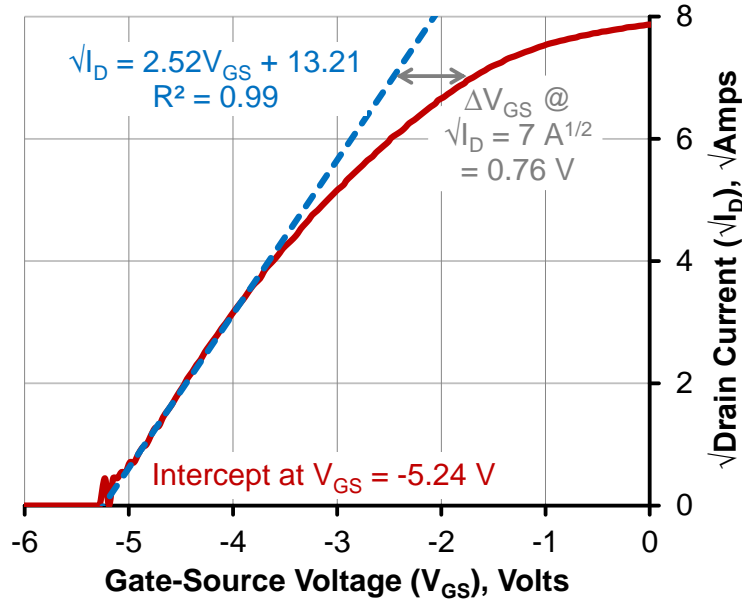


Figure 4.5: $\sqrt{I_D}$ vs V_{GS} relationship for SJDP120R05 SiC JFET, used to calculate VTO, KP and RS parameters

width, which must be assumed to be constant. Although this does not perfectly describe the behaviour of the JFET, the description of its channel behaviour is not adversely affected by this approach. TOX is mostly used for calculating the gain of the transistor and other parameters are responsible for calculating the channel width [177].

The length and width of the channel (L and W) and the lateral diffusion coefficient (LD) are particularly important model parameters. Although L and W appear straightforward to interpret, some care must be taken. The channel width parameter W, having been derived for lateral MOSFETs, represents the half-channel width in the JFET; unlike in the lateral MOSFET, the JFET gate extends both sides of the channel and so pinch-off is effected symmetrically. The definition of L is also different to the lateral MOSFET case. Since the channel is separated from the gate by a depletion region, the effective channel length is slightly longer than the gate depth due to this depletion region extending underneath the P+ gate region.

In this model of the JFET, LD may be used to represent the fact that the effective channel length is much shorter than its theoretical value. As observed by Chen [176], the portion of the channel that extends into the N- drift region as a result of the gate depletion region has a disproportionate effect on the channel behaviour. In particular, the channel is much narrower in this region, due to its lower doping. It is therefore unsurprising that LD should be a significant proportion of L.

Without access to the manufacturer's design parameters, the determination of TOX, L, W and LD can only be based on estimated values. Fortunately, the modelling of similar devices

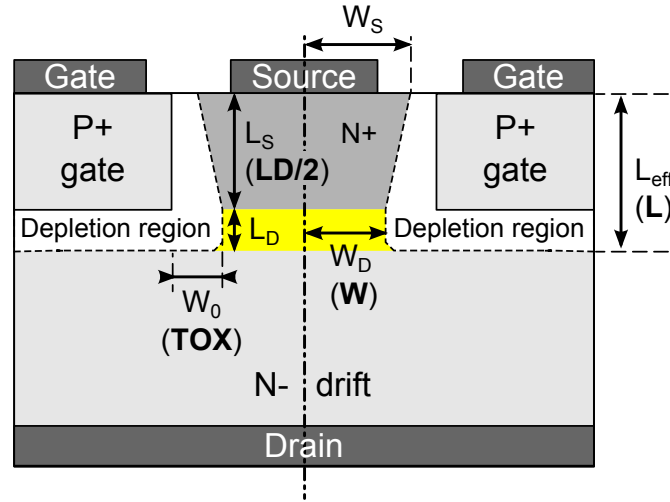


Figure 4.6: Geometric SPICE MOSFET parameters (in bold) and their interpretation for a SiC vertical JFET. The channel region in yellow dominates on-state behaviour, as described by Chen [176].

has been described [176], from which realistic values for these geometric parameters can be estimated. Whilst these authors used normally-off Semisouth parts, enhancement-mode JFETs differ from depletion-mode devices only by their channel width and lower doping density [64].

Using this approach and by making slight adjustments to the extracted values to improve curve fitting, TOX, L, W and LD were estimated to be $0.5 \mu\text{m}$, $2.2 \mu\text{m}$, $1.5 \mu\text{m}$ and $0.9 \mu\text{m}$ respectively.

These geometric parameters are summarised in figure 4.6 which shows the structure of the SiC JFET.

Material properties The behaviour of the semiconductor is represented by three materials parameters: The substrate doping (NSUB), the surface mobility (UO) and the maximum carrier velocity (VMAX). Although its precise value was unknown, NSUB was chosen to be of a fairly typical substrate doping density of $1 \times 10^{16} \text{ cm}^{-3}$, which is in line with doping densities used in similar SiC devices [178].

In conventional MOSFETs, UO is typically somewhat smaller than the bulk mobility due to the presence of traps at the interface. However, as a vertical device with no oxide interface, UO for the JFET is taken to be the same as its bulk mobility of $1000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [179], although the model is reasonably insensitive to its actual value.

VMAX is an important parameter for determining the field-dependent mobility behaviour of the JFET. Although the measured saturation velocity for 4H-SiC of $2 \times 10^5 \text{ ms}^{-1}$ was a useful starting point for determining VMAX, in practice the simulated device behaved as if

its saturation voltage was slightly lower at $1 \times 10^5 \text{ ms}^{-1}$. This small discrepancy may be explained by either the empirical nature of this model or by slightly non-ideal device properties.

Empirical and unknown parameters Several empirical parameters are included in the MOS3 model to aid in fitting the model to experimental data. Two of these, GAMMA and ETA are relevant only to sub-threshold operation and are thus irrelevant to this model. Both these parameters were therefore set to 0.

Three tuning parameters, DELTA, THETA and KAPPA determine the magnitude of the effects of channel width on the threshold voltage, mobility modulation and the saturation field. These were found by iterative curve fitting, having determined all other parameters. The surface inversion potential PHI is not directly applicable to JFETs which do not have an inversion layer. However, PHI must be defined for other parameters to be calculated and so this was also found by curve fitting at the same time as the tuning parameters.

As a result of the curve fitting process, DELTA, THETA, KAPPA and PHI were estimated as 1.12, 0.1, 1 and 0.15 respectively.

4.4.6.3 Summary of MOS3 parameters

A complete list of the MOS3 parameters used in this SPICE model is given in table 4.1.

4.4.6.4 Comparison with experimental measurements

The I-V characteristics for the JFET predicted by the MOS3 model are compared with experimental measurements in figure 4.7. The fit between model and experiment is greatly improved compared to the Semisouth SPICE model and there is very good agreement over the full range of V_{GS} and V_{DS} . Discrepancies between the model and the experiment are greatest near the boundary of the linear and saturation regions, which is likely to be explained by a combination of a lack of consideration of sub-threshold effects and incomplete knowledge of geometric, doping and materials parameters.

Confidence in the MOS3 model of the JFET static performance is further enhanced by figure 4.8, in which the JFET I-V characteristics are plotted over almost the entire voltage range of the device. Behaviour is predictable and consistent over the entire voltage range, whilst the decreasing gradient of the curves with increasing V_{DS} suggests that any errors in model predictions of behaviour at high V_{DS} are likely to be acceptably small.

Experimental validation of figure 4.8 at V_{DS} greater than already investigated is not practicable, due to the exceptionally high instantaneous power that would be required during the

Parameter name	Description	Value	Units
LEVEL	Model level	3	-
VTO	Threshold voltage	-5.24	V
KP	Transconductance parameter	18.6	-
PHI	Surface inversion potential	0.15	V
RD	Drain ohmic resistance	0.049	Ω
RS	Source ohmic resistance	0.015	Ω
IS	Bulk junction saturation current	0	A
NSUB	Substrate doping	1×10^{16}	cm^{-3}
TOX	Oxide thickness	5×10^{-7}	m
TPG	Type of gate material	0	-
L	Channel length	2.2×10^{-6}	m
W	Channel width	1.5×10^{-6}	m
LD	Lateral diffusion	9×10^{-7}	m
UO	Surface mobility	1000	$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$
VMAX	Maximum carrier drift velocity	1×10^5	ms^{-1}
DELTA	Width effect on threshold voltage	1.12	-
THETA	Mobility modulation	1	-
KAPPA	Saturation field	0.1	-

Table 4.1: List of SPICE parameters for MOS3 model for modelling vertical JFET. Unused values are only listed if they do not default to zero.

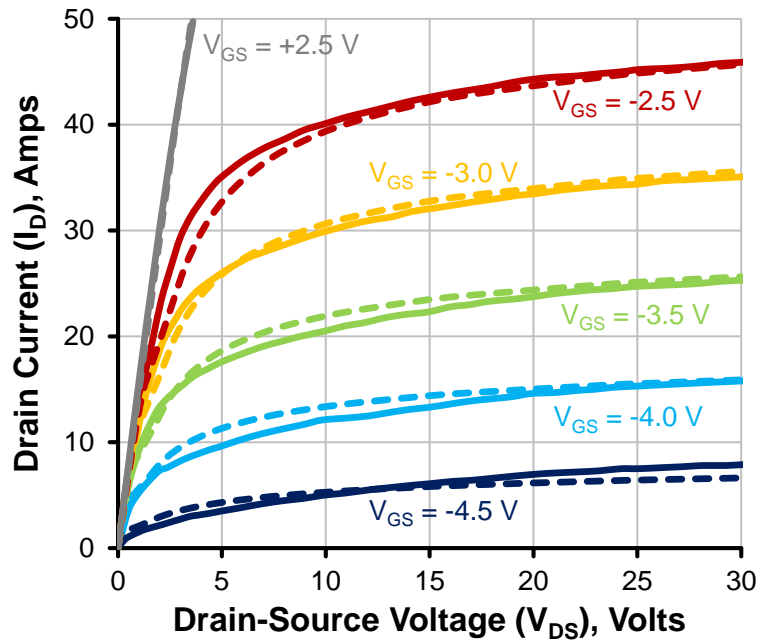


Figure 4.7: I-V curve from experimental measurements (solid lines) vs. MOS3-based SPICE simulations (dashed lines) for Semisouth SJDP120R085 SiC JFET

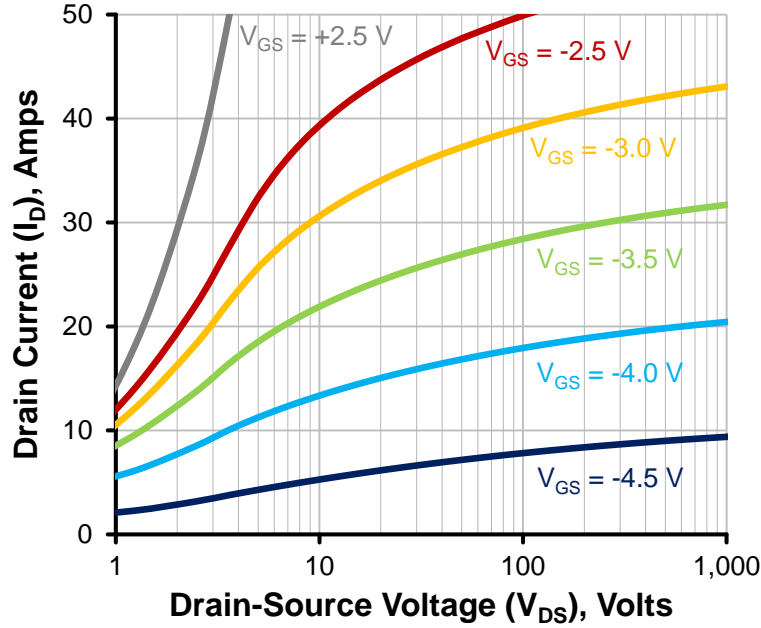


Figure 4.8: I-V curve from MOS3-based SPICE model of Semisouth SJDP120R085 SiC JFET, for V_{DS} of 1 - 1000 V

measurement period. This could easily exceed 100 kW for the fully-enhanced device, even at half its rated V_{DS} .

4.4.7 Capacitance modelling

4.4.7.1 The VDMOS model

Given the unsuitability of the MOS3 model for modelling vertical device capacitances, an alternative model is required. The VDMOS model, intended to model the behaviour of vertical double diffused power MOSFET transistors is such an alternative [180]. It includes an empirically-derived capacitance equation specifically designed to efficiently model capacitance effects in vertical devices, in which C_{DG} changes as a function of $\tanh(V_{GD})$ when forward biased and as a function of $\arctan(V_{GD})$ when reverse biased. V_{GS} is assumed to be constant under all conditions.

4.4.7.2 Capacitance parameters

The only capacitance parameters required for this model are C_{GS} , C_{GDMIN} , C_{GDMAX} and A , which represent the (constant) C_{GS} , the maximum and minimum values of C_{DG} and a curve-fitting parameter respectively. The first two parameters are readily obtained from the device datasheet [79], whilst C_{GDMAX} and A can be determined by curve-fitting the simulated

Parameter name	Description	Value	Units
VTO	Threshold voltage	1,500	V
KP	Transconductance parameter	0	-
CGS	Gate-source capacitance	175×10^{-12}	F
CGDMAX	Maximum non-linear gate-drain capacitance	2.2×10^{-9}	F
CGDMIN	Minimum non-linear gate-drain capacitance	25×10^{-12}	F
A	Non-linear gate-drain capacitance parameter	0.15	-
IS	Body diode saturation current	0	A
VJ	Body diode junction potential	1,500	V
RB	Body diode ohmic resistance	1×10^9	Ω

Table 4.2: List of SPICE parameters for VDMOS model for modelling vertical JFET capacitances. Unused values are only listed if they do not default to zero [180].

device capacitances to the datasheet capacitance curves. In this case the optimum values were found to be: CGS = 175 pF, CGDMIN = 25 pF, CGDMAX = 2.2 nF and A = 0.15.

4.4.7.3 Elimination of other device behaviour

It is important that the remaining aspects of this MOSFET model are disabled. The model itself is too simplistic to accurately model the short-channel effects of the JFET and so the effect of its channel, body diode and parasitic resistances must be eliminated to avoid interference with the MOS3 model.

The effect of the channel is removed by setting the threshold voltage (VTO) higher than the device rating at 1.5 kV and the transconductance parameter (KP) to zero. Similarly, the body diode saturation current (IS) is set to zero, whilst its series resistance (RB) is set to 1 G Ω and its forward voltage set in excess of the device rating at 1.5 kV. All other parameters including the device parasitic resistances and the body diode junction capacitance then either default to zero or are rendered irrelevant. As with the MOS3 model, the nominal temperature is not explicitly specified, but defaults to 27 °C.

4.4.7.4 Summary of VDMOS capacitance model parameters

A complete list of the parameters used in the VDMOS SPICE model is given in table 4.2.

4.4.7.5 Comparison with experimental device data

The device capacitances predicted by the VDMOS capacitance model are compared with experimental values from the device datasheet in figure 4.9. There is extremely good agreement between the model and experimental measurements over the entire voltage range.

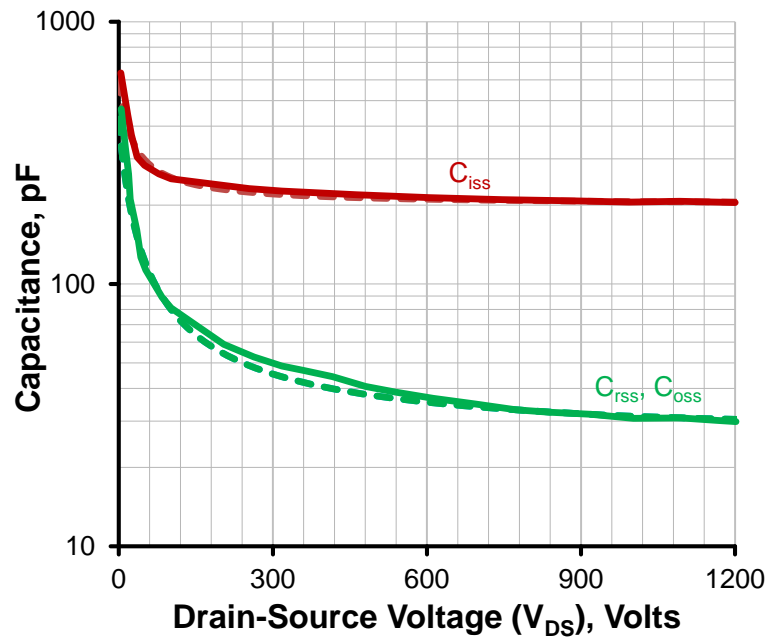


Figure 4.9: Parasitic capacitance vs V_{DS} from datasheet curves (solid lines) vs. VDMOS capacitance model SPICE simulations (dashed lines) for Semisouth SJDP120R085 SiC JFET

4.4.8 Modelling the gate diodes

4.4.8.1 Available diode models

Neither the MOS3 or VDMOS models describe the behaviour of the JFET gate-drain and gate-source diodes, so these must be modelled separately. Fortunately, since the capacitance behaviour of the JFET has already been accounted for, it is not necessary to separately consider the junction capacitance of these diodes.

LTSPICE includes two diode models: the standard Berkeley SPICE model and an idealised model. The standard SPICE model includes much greater detail than is required for modelling the diodes in this case, so the idealised model is used.

4.4.8.2 Diode parameters

The idealised diode model defines separate performance parameters for forward and reverse conduction and the off-state [180]. R_{ON} , R_{REV} and R_{OFF} describe the diode resistance in each of these states respectively, whilst V_{FWD} and V_{REV} represent the forward conduction voltage and reverse breakdown voltages.

Although the idealised diode model is essentially linear, it is capable of describing the non-linear behaviour of the diode as it transitions from the non-conducting to forward or reverse conduction states. The parameters ϵ and ϵ_{REV} define the voltage over

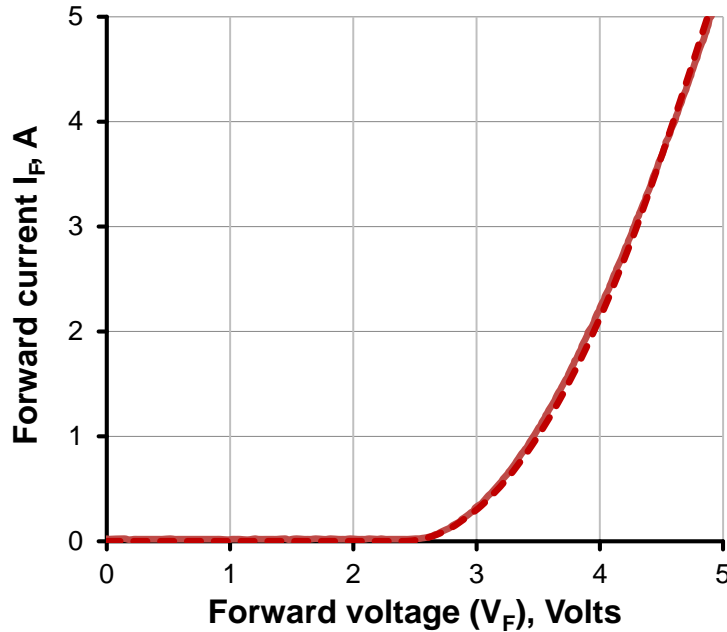


Figure 4.10: Comparison of experimentally measured gate-source/gate-drain diode characteristics (solid line) with idealised SPICE model (dashed line). Measurements for the gate-source and gate-drain diodes were so similar as to be indistinguishable.

which this transition occurs. It is also possible to specify both a forward and reverse current limit using the parameters $ILIMIT$ and $REVLIMIT$.

4.4.8.3 Parameter extraction

The forward conduction parameters were determined by curve-fitting to experimentally measured data (figure 4.10). Both the gate-source and gate-drain diodes had indistinguishable forward conduction characteristics and a very good fit was found with parameter values of $VFWD=2.4$, $RON=0.28$ and $EPSILON=2.15$.

The reverse conduction behaviour of the two diodes is very different. The reverse breakdown voltage of the gate-drain diode must obviously be larger than that of the rated device voltage to avoid breakdown currents flowing from the drain to the gate under normal operation. Since drain-source breakdown behaviour for the JFET is not considered in this model, the reverse breakdown voltage $VREV$ for the gate-drain diode is allowed to default to infinity, rendering $RREV$ and $REVEPSILON$ irrelevant.

The gate-source diode reverse breakdown voltage is much lower than that of the gate-source diode. Reverse conduction occurs due to avalanche breakdown, so a significant variation in $VREV$ may be expected between devices. Constructing a very precise model of gate-source diode breakdown behaviour is therefore not particularly useful. Previous curve

Parameter	Description	Value (G-D)	Value (G-S)	Units
RON	Forward conduction resistance	0.28	0.28	Ω
ROFF	Off-state resistance	0.28	0.28	Ω
VFWD	Diode forward voltage	2.4	2.4	V
VREV	Reverse breakdown voltage	∞	22	V
RREV	Reverse breakdown resistance	∞	0.28	Ω
EPSILON	Quadratic region width	2.15	2.15	V

Table 4.3: List of SPICE parameters for idealised diode model for modelling vertical JFET gate-drain (G-D) and gate-source (G-S) diodes [180]. Unused values are only listed if they are not ignored by default.

tracer measurements on the SJDP120R085 JFET gate-source diode have shown that a reverse breakdown voltage of -22 V is typical. Avalanche breakdown of the gate-source junction is therefore modelled as a simple transition from the blocking region to a linear reverse conduction region of identical resistance to that of forward conduction with VREV=22, RREV=0.28 and REVEPSILON=0.

4.4.8.4 Summary of VDMOS capacitance model parameters

A complete list of the parameters used in the diode SPICE model is given in table 4.3.

4.4.8.5 Comparison with experimental measurements

The forward conduction characteristics of the gate-source and gate-drain from the idealised SPICE diode model are compared with experimental measurements in figure 4.10. Despite a very simple model being used, both simulation and experiment are in close agreement.

4.4.9 Complete hybrid JFET model

The complete hybrid SPICE model of the SiC JFET is assembled from the individual models described above. The MOS3 ‘Channel’ model and VDMOS ‘Capmodel’ capacitance model are connected in parallel. Since the drain and source resistances affect all components of the model, RD and RS are set to zero in the ‘Channel’ model and instead represented as discrete resistances at the drain and source of the the hybrid device respectively. Stray inductance is deliberately excluded from the model, since it has been accurately characterised for the PCB and will therefore be added externally to the SiC JFET.

One interesting feature of the SiC JFET that is apparent from its datasheet [79] is its internal gate resistance. Under normal operation, this is specified as having a typical value

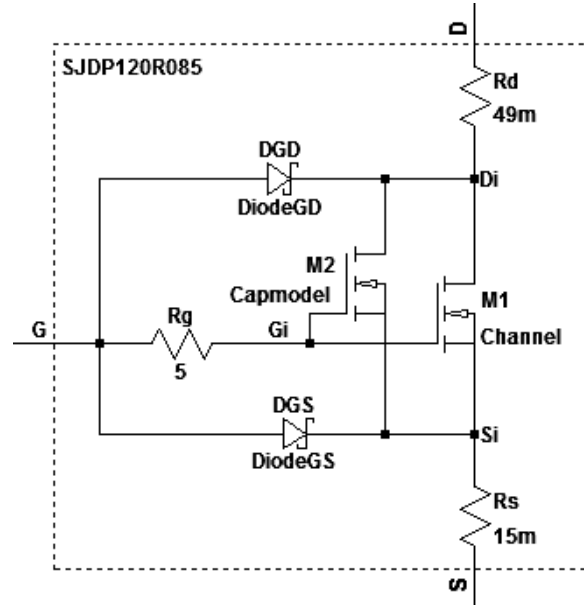


Figure 4.11: Hybrid SPICE model of SJDP120R085 JFET as implemented in LTSPICE

of $5\ \Omega$ and is therefore represented by a discrete resistor in the hybrid model. However, for $V_{GS} > 2.7\text{ V}$, the gate resistance is specified as having a typical value of $0.5\ \Omega$.

This implies that when forward biased the gate-source diode must bypass the internal gate resistance, with current limited only by the diode forward resistance. Indeed, the estimated forward resistance of $0.28\ \Omega$ is in line with the typical value of $0.5\ \Omega$ quoted in the datasheet. Given the extremely similar forward characteristics of both gate diodes, both must bypass the $5\ \Omega$ internal gate resistance of the JFET. This is a credible interpretation, because the trench gate structure of the JFET means that its gate metallisation is much closer to the substrate than to the source metallisation [76].

The schematic of the complete hybrid model is shown in figure 4.11.

4.4.10 SiC JFET modelling conclusions

Modelling a SiC vertical JFET presents unusual challenges due to its vertical geometry and susceptibility to short-channel effects. Due to the significant limitations of the built-in SPICE JFET model, this device has instead been modelled by constructing a hybrid SPICE model based on native MOSFET models and discrete components. By careful manipulation of model parameters, the hybrid model has been shown to accurately describe both the static and dynamic characteristics of the SiC JFET. A complete SPICE subcircuit for the hybrid SiC JFET model is given in appendix B.

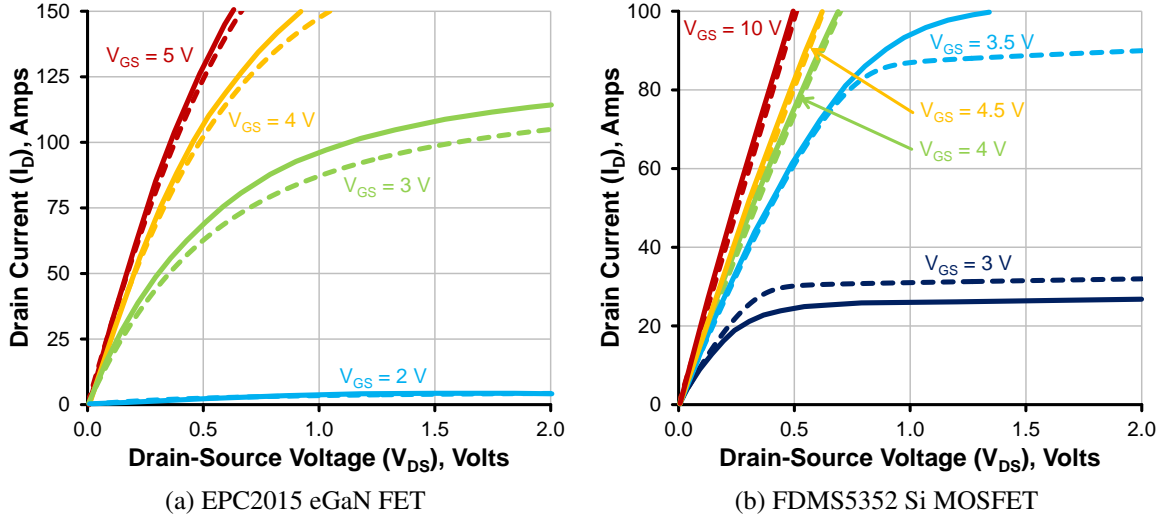


Figure 4.12: I-V curves from datasheet figures (solid lines) compared to SPICE simulation results (dashed lines) for LV transistors [170, 171]

4.5 Modelling a SiC JFET cascode

4.5.1 LV device models

Sophisticated device models were available from the manufacturers of both the LV transistors used in this work [181, 182]. The FDMS5352 model is based on a level 7 MOSFET model with additional subcircuit components, whilst the EPC2015 is modelled using a subcircuit consisting of behavioural current sources and non-linear capacitances that directly implement a mathematical model of the devices.

To validate the models, I-V and C-V curves produced by the device models are compared against the characteristics described in the device datasheets in figures 4.12 and 4.13. There is generally good agreement between the SPICE models and datasheet figures over the range of V_{DS} and V_{GS} , with some minor discrepancies. The FDM5352 SPICE model required minor adjustments to improve its fit, with the threshold voltage V_{TO} being decreased from 2.24 to 2.15 V whilst the drain resistance was reduced from 3.9 to 2.3 $m\Omega$. These adjustments are well within normal process variation for this device, with V_T , for example, being specified by the manufacturer to be with a range of 1.0 to 3.0 V.

Despite some variation compared to the datasheet figures, these manufacturers' SPICE models show close enough agreement to quoted device specifications for them to be useful in constructing a SPICE model of a cascode circuit.

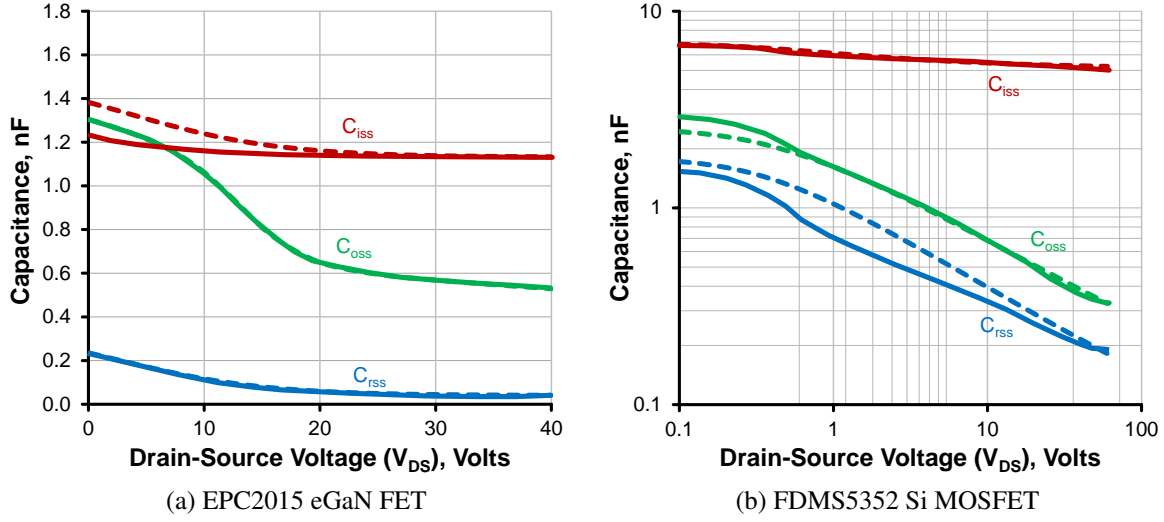


Figure 4.13: Parasitic capacitance vs V_{DS} from datasheet figures (solid lines) compared to SPICE simulation results (dashed lines) for LV transistors [170, 171]

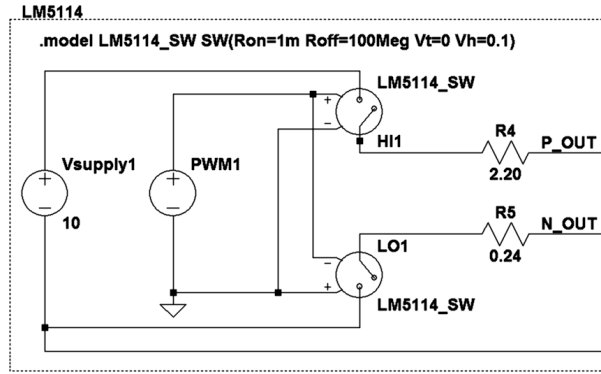


Figure 4.14: SPICE representation of SOT-23 LM5114 gate driver

4.5.2 Gate driver

The LM5114 gate driver used in the experimental work described in chapter 6 was simulated as a subcircuit. Its complementary MOS outputs were represented by two voltage controlled switches, controlled by a voltage source. The gate driver power supply was represented by a simple DC voltage source. This arrangement allowed arbitrary pulse-width modulation (PWM) signals to be supplied by the gate driver. The internal resistance of the gate driver outputs was simulated based on typical characteristics quoted in the datasheet [183]. Three external connections to the subcircuit were provided: A positive and negative drive output and a ground reference for connecting to the driven MOSFET's source. The gate driver subcircuit is shown in figure 4.14.

4.5.3 Clamped inductive load and circuit parasitics

To make direct comparisons between the model and experimental results, a clamped inductive load was simulated. This was modelled as a 25 A constant current source with an inverse parallel free-wheel diode, connected to a 600 V DC bus supplied by an ideal voltage source. The current source is a simplified representation of the 100 μH power inductor used in the experimental measurements, but this is not detrimental to the model. Even with the full DC bus voltage imposed across it, the inductor current changes only by the order of 2 % over a typical 100 ns switching period at rated current (25 A). Its inductance is also at least three orders of magnitude greater than any parasitic inductances, making its behaviour close to that of an ideal current source.

The C4D10120 SiC Schottky free-wheel diode is modelled using a SPICE model provided by the manufacturer [184]. This model includes the effect of the voltage-dependent junction capacitance, which is important for modelling capacitive reverse recovery effects.

Previous work has shown that the inductance between the HV source and LV drain ($L_{S(HV)}$) is significant during switching [185]. This is therefore included in the SPICE model. Its value was estimated as 7.5 nH for a HV transistor in a TO-247 package. This was calculated by matching the rise time of I_D between simulation and experiment, since this is a condition in which the voltage across the inductor is well defined as $V_{L(S,HV)} = V_{bias} + V_{T(HV)}$.

In general, stray inductance in other locations has been found not to greatly influence the switching process [185], although it can contribute to parasitic oscillations. An exception to this is the LV source inductance ($L_{S(LV)}$), which also influences current rise and fall times. However, this is considered to be much smaller than $L_{S(HV)}$ due to the low inductance packaging of the LV transistors and is therefore not considered separately. Stray inductance in other locations are not included. Parasitic capacitances in the PCB are also not considered in this analysis since their behaviour is strongly layout dependent.

The complete SPICE SiC JFET cascode clamped inductive load model is shown in figure 4.15.

4.6 Validating the SPICE model

The cascode hard-switching SPICE model was compared with experimental measurements of a SiC JFET/Si MOSFET cascode based on the SJDP120R085 and FDMS5352 devices. Measurements were taken for clamped inductive switching at 25 A and 600 V. This cascode used gate resistances of $R_{GH(LV)} = 0 \Omega$, $R_{GL(LV)} = 4.7 \Omega$ and $R_{G(HV)} = 1 \Omega$ to give rapid, but well controlled switching. Switching waveforms for the model and experimental measurements are compared directly in figure 4.16.

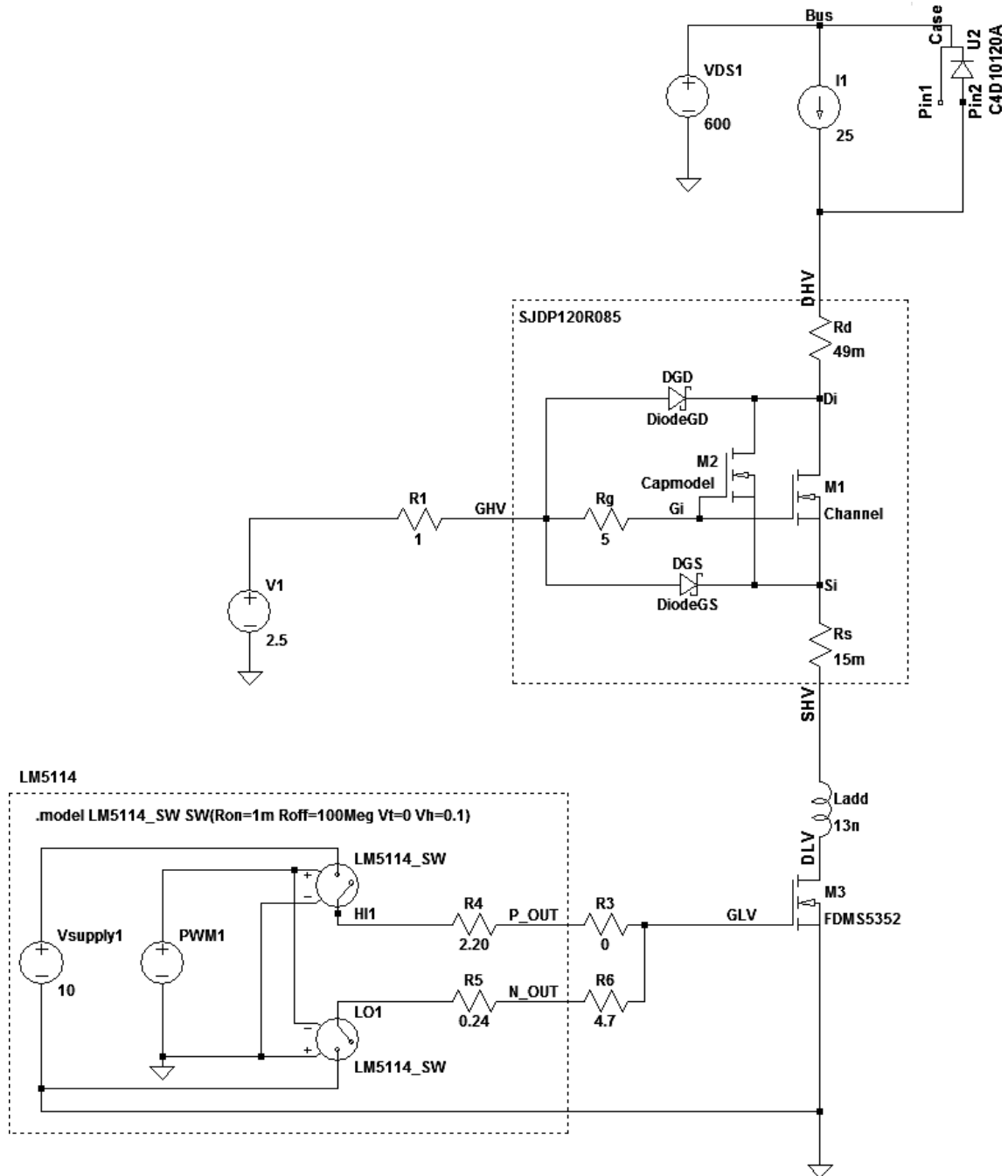


Figure 4.15: Complete SPICE SiC JFET cascode clamped inductive load model

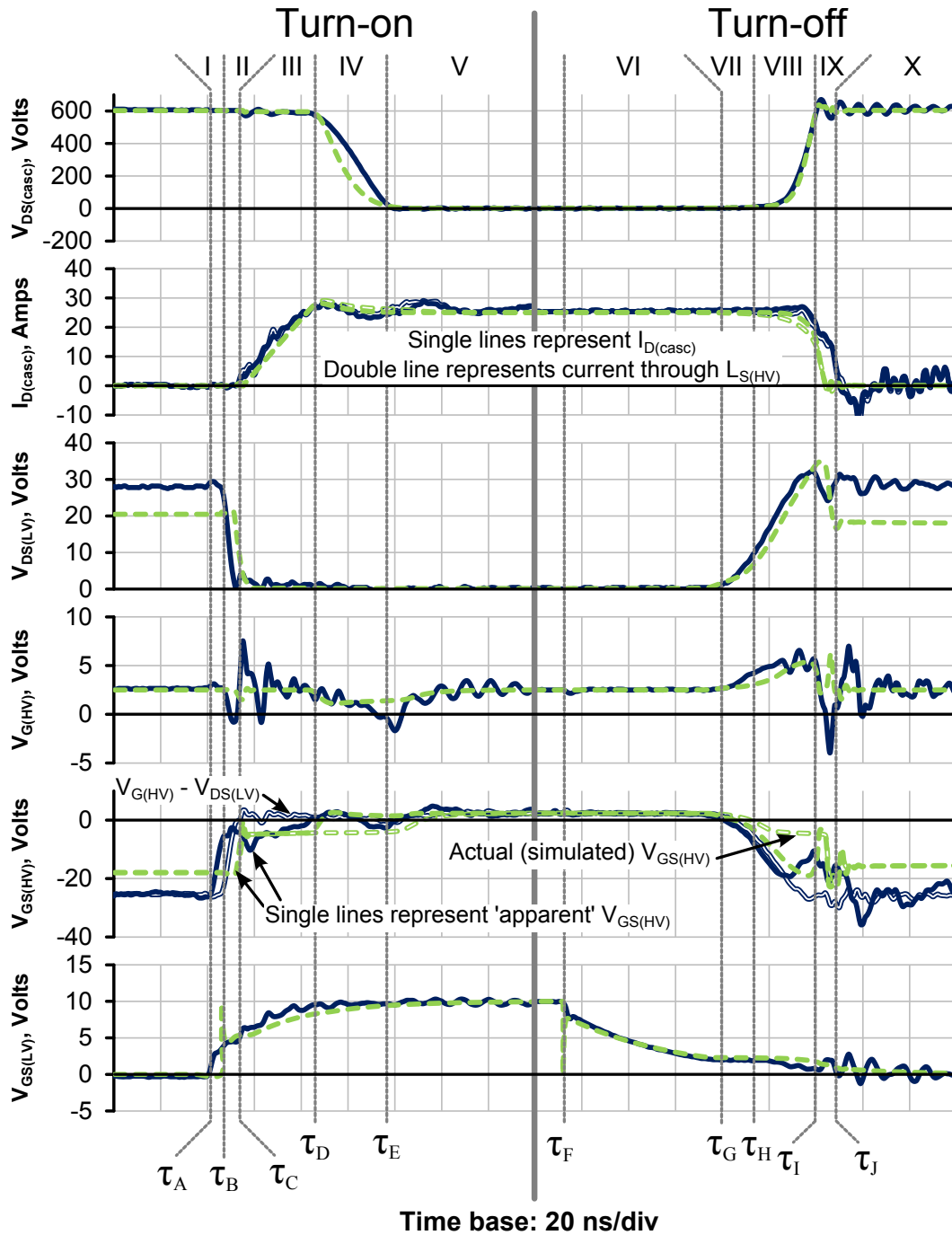


Figure 4.16: Turn-on and turn-off behaviour of a SiC JFET cascode. Blue lines represent experimental measurements and green lines represent the SPICE model

4.6.1 Model performance

In general figure 4.16 shows a good match between measurement and SPICE simulation, particularly at turn-off. There are, however a few interesting anomalies.

4.6.1.1 Stray capacitance at C_{DG}

The changes in $V_{DS(casc)}$ and $I_{D(casc)}$ generally show a good fit between simulation and experiment. However, the SPICE model predicts a faster initial fall of $V_{DS(casc)}$, followed by a more pronounced reduction in $\frac{dV_{DS(casc)}}{dt}$ compared to the experimental measurements. This is likely to be caused by stray capacitance in the test PCB in parallel with $C_{DG(HV)}$, which is not accounted for in the model. This will cause a proportionally significant increase $C_{oss(casc)}$ at high voltages, leading to the more linear decrease in $V_{DS(casc)}$ visible in the experimental measurements. More accurate simulations should therefore be possible if PCB capacitance is characterised and included in the simulation.

4.6.1.2 Variations in gate diode breakdown and stray capacitance parallel to LV transistor

There is a discrepancy between the simulated and measured values of $V_{DS(LV)}$ in the off-state. $V_{GS(HV)}$ is also affected, as it has a strong dependence on the value of $V_{DS(LV)}$.

This happens for two reasons. The off-state value of $V_{DS(LV)}$ is set by a transient redistribution of charge at the point that $I_{D(casc)}$ falls to zero, which is explained in section 4.9.2. As this happens, $V_{GS(HV)}$ falls rapidly, which may cause the HV gate-source diode to briefly enter avalanche breakdown. In the SPICE model, the breakdown voltage of this diode is set at -22 V, but this value varies considerably between devices; the JFET used for the experimental set-up may have had a larger breakdown $V_{GS(HV)}$. Secondly, the eventual value of $V_{DS(LV)}$ is strongly dependent on $C_{oss(LV)}$. Stray PCB capacitance in parallel to the LV transistor will therefore increase the final value of $V_{DS(LV)}$.

4.6.1.3 Gate behaviour

Because passive voltage probes are used for measurement in this work, $V_{GS(HV)}$ cannot be measured directly. Whilst it can be estimated to be $V_{GS(HV)} \approx V_{G(HV)} - V_{DS(LV)}$, such a measurement also includes any voltage drops across $R_{G(HV,int)}$ and $L_{S(HV)}$. As the effect of the transistor internal resistance cannot be removed from terminal measurements of the transistor, the ‘true’ value of $V_{GS(HV)}$, which governs transistor switching behaviour, is impossible to measure directly.

This makes it difficult to properly observe the HV gate behaviour from experimental switching measurements, since effects such as the Miller plateau are obscured. This is particularly true during cascode turn-off when the Miller current is not constant as $V_{DS(casc)}$ rises. This is not a problem in the SPICE model, where the internal HV transistor gate behaviour can be directly probed.

To give a simple comparison between experimental and simulation $V_{GS(HV)}$ measurements, the ‘apparent’ value of $V_{GS(HV)}$ at the HV transistor terminals is used. This includes the effect of $R_{G(HV,int)}$ but excludes the effects of $L_{S(HV)}$. For the experimental measurements, for which a direct HV transistor source voltage measurement was not possible, this is calculated as $V_{GS(HV,apparent)} = V_{G(HV)} - V_{DS(LV)} - \frac{d}{dt} \left(I_{D(casc)} - \frac{V_{G(HV)} - V_{bias}}{R_{G(HV)}} \right) \cdot L_{S(HV)}$. To minimise noise in the numerical differentiation, exponential smoothing was applied to the current terms, using a time constant of 10 ns to match the rise time of the Rogowski coil. The ‘apparent’ $V_{GS(HV)}$ was measured directly in the SPICE simulation.

In addition, waveforms for the experimental measurement of $V_{G(HV)} - V_{DS(LV)}$ and for the simulated ‘true’ value of internal $V_{GS(HV)}$ are included in figure 4.16 to show the difference between these measurements.

There is generally a good fit between the measured and simulated gate characteristics for both HV and LV devices. Despite the measurement difficulties, there is a good match between the ‘apparent’ $V_{GS(HV)}$ measurements and simulations. The noise and parasitic oscillations visible only in the experimental traces are likely to be examples of the limitations of the experimental measurements, rather than of the SPICE model.

4.6.2 Conclusion

The SPICE model developed in the previous section has been shown to be capable of simulating a real cascode circuit to a good degree of accuracy at all nodes in the circuit. This makes it useful as a tool for investigating the effect of different circuit parameters on cascode switching behaviour in simulation.

4.7 Simplifying the switching model

4.7.1 The need for a simple analytical model

The SPICE model of the cascode switch developed in the previous section is a helpful tool for investigating HV SiC JFET cascode circuits. However, it is highly device specific and requires considerable development effort, particularly when suitable device models are not readily available.

SPICE modelling quickly becomes impractical as an aid to device selection, due to the number of possible permutations and does not provide a clear insight into the effect of circuit parameters on the switching process. This makes it a cumbersome method of optimising specific design parameters. A simple, idealised model of cascode hard-switching is therefore desirable as a way of quickly optimising cascode design.

As previously described in section 2.8.4, some authors have sought to model aspects of cascode switching behaviour. However, to date, no simple analytical models of cascode switching have been derived that are suitable tools for cascode circuit design. A number of simple cascode performance improvements have also been overlooked in previous work.

It has already been shown that the use of a positive HV gate bias can reduce on-state switching losses [185] and also allows the cascode configuration to be applied to enhancement mode HV transistors [114]. Consideration of HV gate resistance is also important. The presence of a HV gate resistor gives greater control over the switching process and reduces parasitic oscillations [185]. A HV gate resistance must also be considered to account for the often significant internal gate resistance of HV power devices. The implications of these approaches can be more easily explored using a simplified switching model.

To achieve the required simplicity, a series of assumptions and simplifications of circuit behaviour will be used to describe the dominant processes during each stage of switching. From this, a set of equations to describe the behaviour of various device voltages and currents will be derived. These will be used to formulate a set of equations to estimate key performance parameters, which will aid device selection and help with the creation of design guidelines for cascode circuits

4.7.2 Basis of the simplified model

The simplified analytical model is based on an analysis of similar hard-switching conditions to those described in section 4.4.9. Switching behaviour is assumed throughout to be governed by circuit level (rather than semiconductor level) effects.

The key parameters in this model are the transistor gate resistances, the parasitic device capacitances and the stray inductance between the two devices. Additionally, the voltage sources driving the HV and LV gates, the gate-source threshold voltages of the two transistors and the current and voltage operating conditions of the clamped inductive load are relevant. These key parameters are shown in figure 4.17. It is assumed that this cascode circuit operates in a clamped inductive load circuit similar to that of figure 3.5 with load current I_L , DC bus voltage V_{DC} and an ideal free-wheel diode.

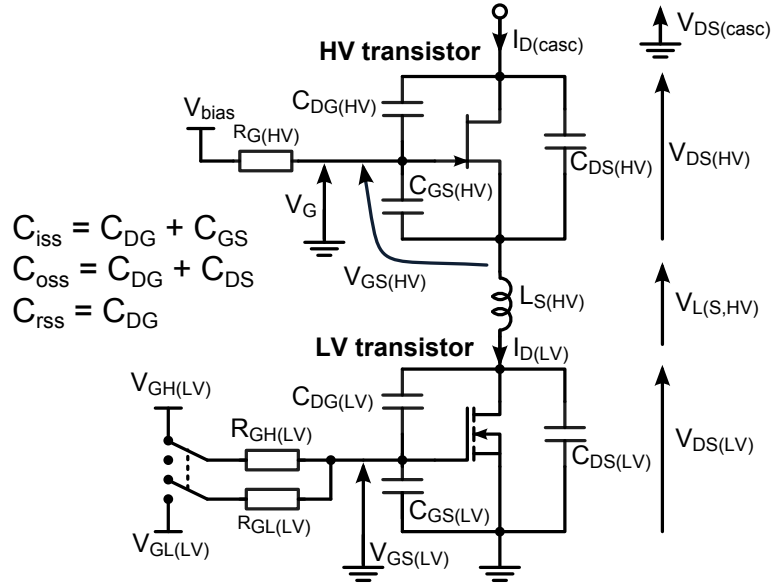


Figure 4.17: Schematic of cascode circuit used for simplified model

4.8 Modelling assumptions

To describe the switching behaviour of the cascode circuit with a set of simple equations, the switching period must be broken down into a series of discrete stages and device behaviour idealised. To do this, a series of simplifying assumptions are used:

4.8.1 Turn-on

At turn-on, the LV transistor is assumed to be switched as quickly as possible. Current rise is then controlled solely by the voltage ($V_{bias} - V_{T(HV)}$) imposed across stray inductance between the two devices ($L_{S(HV)}$) and is therefore linear.

4.8.2 Parasitics

The only parasitics considered are the internal stray capacitances of the devices (C_{iss} , C_{oss} , C_{rss}) and $L_{S(HV)}$. Other stray capacitances are not included since they are heavily dependent on layout and should not have a major impact in a carefully designed circuit. It is also assumed that C_{rss} of both devices is much smaller than C_{iss} or C_{oss} , such that a change of gate voltage cannot directly cause a significant change in drain-source voltage.

	HV (SJDP120R085)	LV (FDMS5352)
Quoted typical threshold voltage (V_T)	-5	1.8
Voltage at which max. g_m reached (S)	-4.5	2.5
Approx max. g_m (S)	9	45

Table 4.4: Comparison between datasheet threshold voltage and voltage at which peak g_m reached [79, 171].

4.8.3 Device operation

Both transistors are assumed to operate entirely in their saturation region, except when fully on. In the on-state, they are assumed to operate in their linear region, with negligible channel resistance and hence negligible V_{DS} .

4.8.4 Transconductance

Both device transconductances (g_m) are assumed to be sufficiently high ($\rightarrow \infty$) that the gate-source voltage is held approximately constant at V_T whilst the transistors switch (since $I_D = g_m(V_{GS} - V_T)$ in the saturation region).

In reality, g_m varies with gate voltage, only reaching a peak value some time after the threshold voltage has been exceeded. Experimental measurements on typical devices show a disparity between the quoted threshold voltage and voltage at which g_m reaches its maximum (table 4.4). These figures suggest that better predictions may be obtained from the idealised model if these values are used instead of datasheet values, which are measured at low current.

4.8.5 Constant capacitance

Parasitic device capacitances are assumed constant. However, in practice, these are dependent on V_{DS} , with both C_{oss} and C_{rss} having an approximately inverse square root relationship with V_{DS} . For simple comparisons between devices and components, this assumption is likely to be adequate. However, for more precise estimates, non-linear expressions for capacitance may be substituted, or calculated numerically.

4.8.6 Step changes

At certain times in the switching process, very rapid changes in voltage occur in the gate loop consisting of $R_{G(HV)}$, $C_{GS(HV)}$, $L_{S(HV)}$ and sometimes $C_{oss(LV)}$. The time constant of this circuit is typically much smaller than the duration of each stage, so these are modelled as step changes of voltage.

4.8.7 External effects

The cascode circuit is capable of producing extremely high $\frac{dV}{dt}$ and $\frac{dI}{dt}$. Stray inductance or poor selection of components in the power circuit may cause oscillations, transients or parasitic effects that are not considered. The effects of diode reverse recovery are also neglected.

4.9 Simplifying the switching model

Both the turn-on and turn-off waveforms are separated into different time periods, each representing a distinct stage of the switching process. The boundary between each time period is described by the parameters τ_A, \dots, τ_J and are shown in figure 4.18.

The behaviour of the cascode in each stage during switching is now described. For each time period, the equivalent circuit is given and the underlying assumptions explained. This is used to derive a set of simplified equations that describe the behaviour of device voltages and currents during each stage. These are summarised in table 4.5.

The equivalent circuit for each stage of switching shows the key circuit components for that period. Current flows are represented by red dashed lines and voltages described in the text are represented by solid blue arrows. Arrowheads represent whether these quantities are increasing or decreasing during the stage.

4.9.1 Turn-on

Stage I ($\tau_A \leq t < \tau_B$) - LV gate voltage rises

At $t = \tau_A$, the LV gate driver voltage rises rapidly from $V_{GL(LV)}$ to $V_{GH(LV)}$. $C_{iss(LV)}$ begins charging through the turn-on resistor ($R_{GH(LV)}$) until the gate voltage ($V_{GS(LV)}$) reaches the threshold voltage ($V_{T(LV)}$).

For transistors for which C_{rss} is a substantial fraction of C_{oss} , this can also lead to a noticeable increase of $V_{DS(LV)}$ due to a displacement current flowing through C_{rss} and charging $C_{DS(LV)} \parallel C_{GS(HV)}$. Under most circumstances, this effect is small compared to the magnitude of $V_{DS(LV)}$ and so it is neglected in this analysis.

This process can be modelled as a simple exponential capacitor charging equation. It is assumed that the LV gate driver voltage rises instantaneously and has zero output impedance, which is a reasonable assumption provided that $R_{GH(LV)} \gg R_{driver}$.

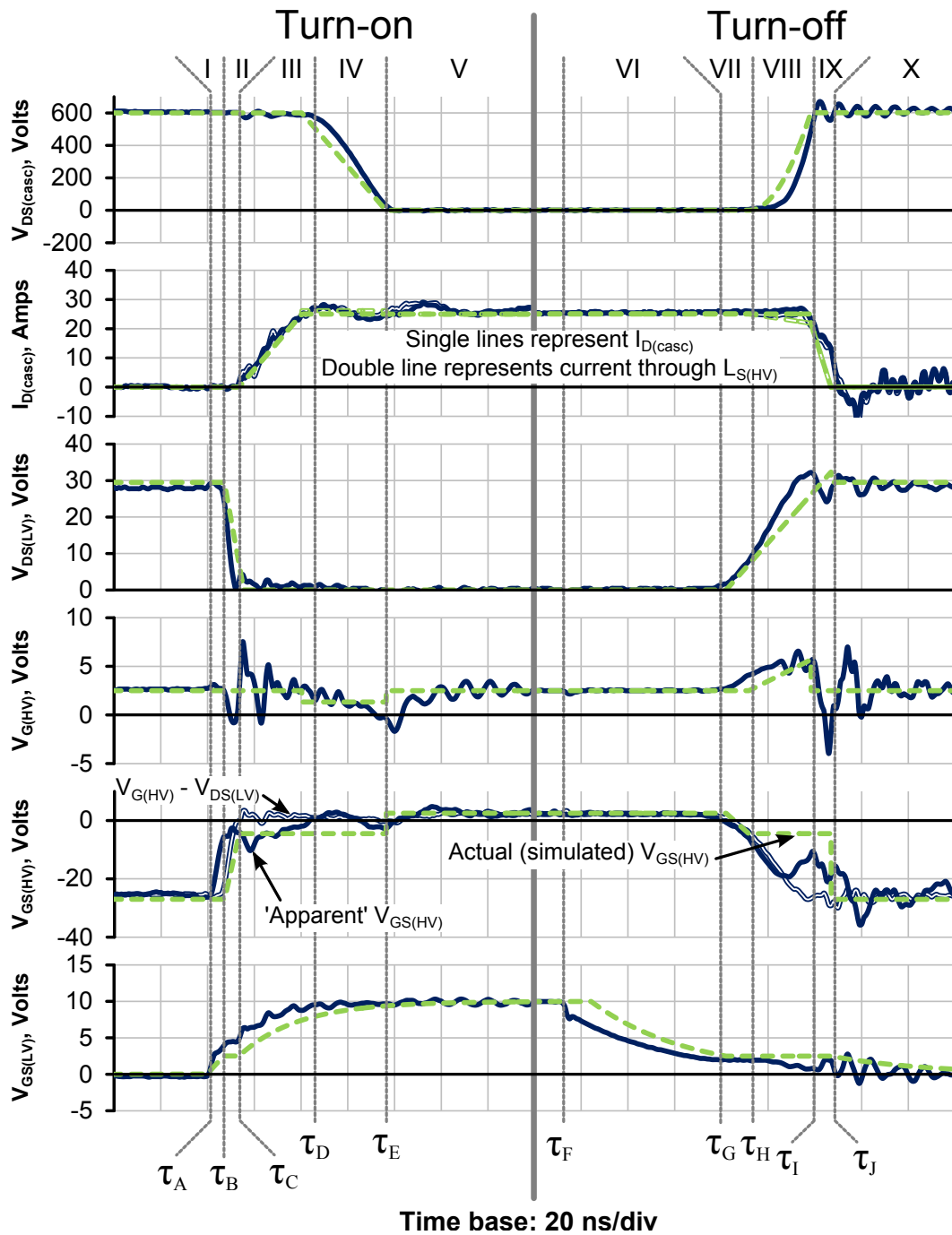


Figure 4.18: Turn-on and turn-off behaviour of a SiC JFET cascode. Blue lines represent experimental measurements and green lines represent the idealised model. Note that dashed line in $V_{GS(HV)}$ is the apparent (measured) value and solid line is the actual value, accounting for voltage across JFET source inductance.

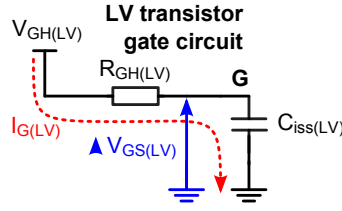


Figure 4.19: Equivalent circuit for stage I

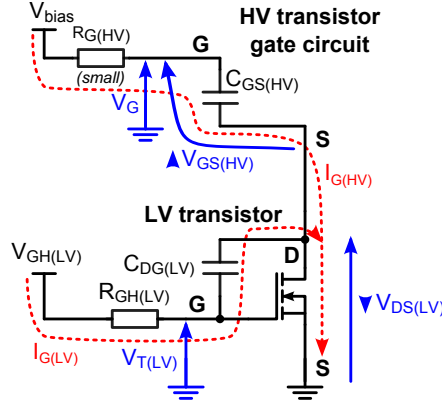


Figure 4.20: Equivalent circuit for stage II

Stage II ($\tau_B \leq t < \tau_C$) - HV gate voltage rises

At $t = \tau_B$, $V_{GS(LV)}$ reaches $V_{T(LV)}$ and the LV transistor starts to turn on. Since the HV transistor remains fully off, the LV transistor does not have to carry any of the load current (I_L). This means that it can switch resistively, rapidly discharging $C_{oss(LV)}$ whilst charging $C_{GS(HV)}$ and causing $V_{DS(LV)}$ to drop.

As $V_{DS(LV)}$ falls, $V_{GS(HV)}$ rises until it reaches $V_{T(HV)}$ at $t = \tau_C$. The rise of $V_{GS(HV)}$ begins slightly after the fall of $V_{DS(LV)}$ due to the time constant of the RLC circuit formed of $R_{G(HV)}$, $C_{GS(HV)}$ and $L_{S(HV)}$. However, in practice this delay is usually negligible and is not included in this model.

The voltage changes during this stage are modelled as linear processes, with $\frac{dV_{DS(LV)}}{dt}$ controlled by $R_{GH(LV)}$ and the LV drain-gate capacitance $C_{DG(LV)}$. $V_{GS(LV)}$ remains clamped at $V_{T(LV)}$ throughout.

It is important that $V_{DS(LV)}$ does not fall too quickly during this stage. If this happens, a disproportionate current flows through $C_{GS(HV)}$, causing a significant voltage drop across $R_{G(HV)}$. This can lead to oscillations in $I_{D(casc)}$. This problem can be alleviated by increasing $C_{DG(LV)}$ or $R_{GH(LV)}$ to reduce $\frac{dV_{DS(LV)}}{dt}$ or by increasing $L_{S(HV)}$ [141].

The turn-on delay for the cascode is given by $t_{d(on)} = \tau_C - \tau_A$. Since it is dependent on the time for the LV transistor to switch resistively, it is typically very short (of the order of a few ns).

Stage III ($\tau_C \leq t < \tau_D$) - Drain current increases

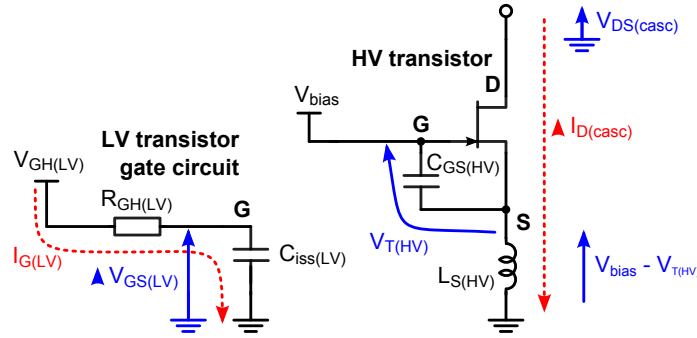


Figure 4.21: Equivalent circuit for stage III

When $V_{GS(HV)}$ reaches $V_{T(HV)}$ at $t = \tau_C$, the HV device begins to turn on, causing the drain current $I_{D(casc)}$ to rise until it is equal to I_L .

Since it is assumed that $V_{DS(LV)}$ falls quickly, the rise of $I_{D(casc)}$ is determined only by $L_{S(HV)}$. Therefore, there is no advantage to having a large value of $R_{GH(LV)}$ and its value is assumed to be small to ensure a rapid fall time for $V_{DS(LV)}$, although a non-zero value does help to damp parasitic oscillations in the LV gate.

$V_{DS(LV)}$ therefore continues to fall rapidly at the beginning of this stage until it reaches zero a short time later, where it remains. Since $V_{DS(LV)}$ is zero for the majority of this stage, it has negligible influence on the rise of $I_{D(LV)}$.

The following part of the stage is unusual: In the conventional linear MOSFET model, it would be assumed that V_{GS} of the HV transistor would continue to rise as in stage II until it reaches a level at which I_L can be supported [186], before reaching a plateau as V_{DS} falls. This cannot happen in this case, since $L_{S(HV)}$ must be considered, having already been shown to be significant [185].

Therefore, as $V_{DS(LV)}$ drops rapidly to zero, the voltage difference between the HV source and LV drain is imposed across $L_{S(HV)}$. Since the HV gate current is negligible at this point, an equilibrium exists such that $V_{L(S,HV)} + V_{GS(HV)} = V_{bias}$. Provided the HV transistor has a reasonably high g_m and hence $V_{GS(LV)} \approx V_{T(HV)}$, an approximately constant voltage of $V_{L(S,HV)} = V_{bias} - V_{T(HV)}$ is applied across the stray inductance.

This has two effects: it leads to a linear rise in $I_{D(casc)}$ due to the constant voltage across the inductor and it also causes the turn-on plateau for $V_{GS(HV)}$ to extend into the current rise period.

Stage IV ($\tau_D \leq t < \tau_E$) - Drain-source voltage falls

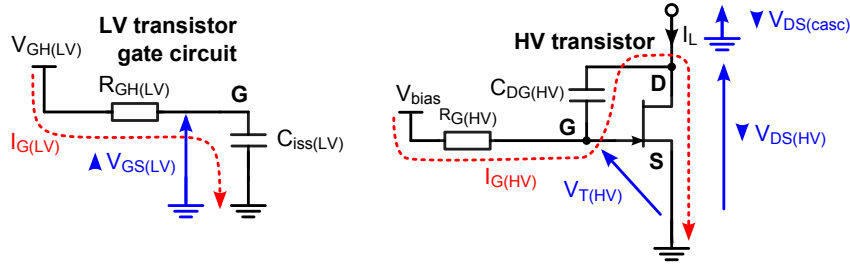


Figure 4.22: Equivalent circuit for stage IV

At $t = \tau_D$, $I_{D(casc)}$ reaches I_L . This enables the current through the free-wheeling diode to drop to zero, although there may be a brief overshoot in $I_{D(casc)}$, depending on the reverse recovery characteristics of the diode [186]. At this point, $V_{DS(casc)}$ is no longer clamped by the free-wheel diode and is able to fall linearly until it reaches zero. The voltage fall is limited by the Miller current, which is set by $V_{T(HV)}$, $R_{G(HV)}$ and $C_{DG(HV)}$.

The effect of the Miller current can be clearly seen in figure 4.18 as the noticeable drop in the $V_{G(HV)}$ waveform for the duration of Stage IV. Since $I_{D(casc)}$ remains clamped at I_L during this period, the Miller current flows through the channels of both devices, causing $I_{S(HV)}$ to increase to $I_{S(HV)} = I_L + I_{miller(HV)}$.

The drop in $V_{G(HV)}$ is assumed to be approximately a step change, since it is not dependent on C_{GS} charging or discharging. Instead, it is caused by the simultaneous effects of Miller current starting to flow through $R_{G(HV)}$ and the voltage across $L_{S(HV)}$ falling to zero, leading to a step change in the voltage at the HV source.

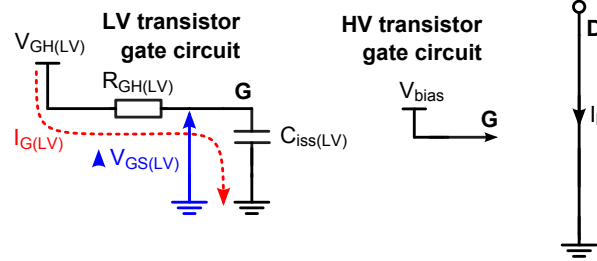
Stage V ($t > \tau_E$) - Fully on

Figure 4.23: Equivalent circuit for stage V

As soon as $V_{DS(casc)}$ reaches zero at $t = \tau_E$, Miller current ceases to flow through $R_{G(HV)}$ and $V_{GS(HV)}$ rises quickly to V_{bias} . This process is modelled as instantaneous, since the time constant $R_{G(HV)}C_{iss(HV)}$ is required to be small for effective operation of the cascode.

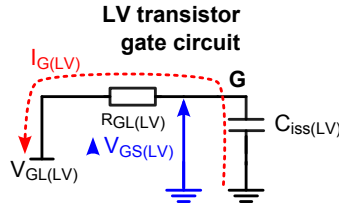
4.9.2 Turn off**Stage VI ($\tau_F \leq t < \tau_G$) - LV gate voltage falls**

Figure 4.24: Equivalent circuit for stage VI

At $t = \tau_F$, the LV gate driver voltage falls rapidly from $V_{GH(LV)}$ to $V_{GL(LV)}$. $C_{iss(LV)}$ begins discharging through $R_{GL(LV)}$ until $V_{GS(LV)}$ falls to $V_{GS(LV)} = V_{T(LV)} + \frac{I_L}{g_{m(HV)}} \approx V_{T(LV)}$. This process is modelled as a simple exponential capacitor discharge equation.

4.9.2.1 Stage VII ($\tau_G \leq t < \tau_H$) - HV gate voltage falls

Once $V_{GS(LV)} \approx V_{T(LV)}$ at time τ_G , the LV transistor starts to turn off. Since g_m is assumed to be large, the gate is clamped at $V_{T(LV)}$ for the duration of this period.

The constant voltage of $V_{T(LV)} - V_{GL(LV)}$ across $R_{GL(LV)}$ sets the Miller current through $C_{DG(LV)}$, leading to a linear rise of $V_{DS(LV)}$. The rise of $V_{DS(LV)}$ leads to a corresponding fall in $V_{GS(HV)}$.

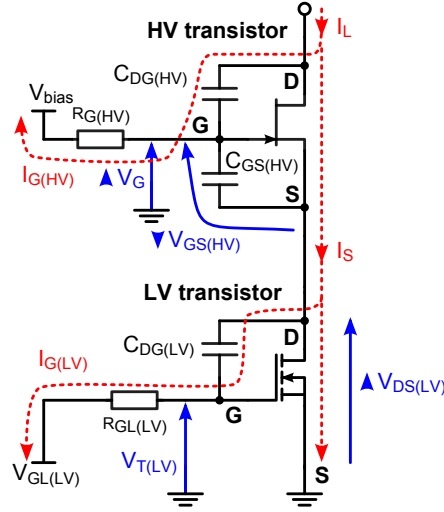


Figure 4.25: Equivalent circuit for stage VII

The linear increase in voltage at the source of the HV transistor also leads to a displacement current of approximately $C_{DG(HV)} \frac{dV_{DS(LV)}}{dt}$ to flow through $R_{G(HV)}$. $C_{DG(HV)}$ may be quite large when $V_{DS(HV)} \approx 0$ and this means that $V_{GS(HV)}$ does not reach $V_{T(HV)}$ at the end of this stage until $V_{DS(LV)} \approx V_{bias} - V_{T(LV)} + R_{G(HV)} C_{DG(HV)} \frac{dV_{DS(LV)}}{dt}$. However, since the $R_{G(HV)} C_{DG(HV)}$ time constant is usually small compared to the duration of this stage, it is neglected in the calculation of $V_{T(LV)}$.

Whilst the increasing $V_{DS(LV)}$ during this stage clearly directly leads to an increase in $V_{DS(casc)}$, its magnitude is small ($\sim 5\%$) compared to V_{DC} . $V_{DS(casc)}$ is therefore assumed to remain at 0 throughout this period.

The cascode turn-off delay is given by $t_{d(off)} = \tau_H - \tau_F$. It is usual for cascode turn-off resistors to need to be much larger than turn-on resistors for optimum switching. The turn-off delay of a cascode is therefore usually much greater than its turn-on delay.

4.9.2.2 Stage VIII ($\tau_H \leq t < \tau_I$) - Drain-source voltage rises

As $V_{GS(HV)}$ reaches $V_{T(LV)}$ at τ_H , the HV transistor begins to turn off, resulting in $V_{GS(HV)}$ being clamped to $V_{T(HV)}$ for the remainder of this period. Since the LV transistor is still operating under approximately maximum current conditions, the linear rise of $V_{DS(LV)}$ continues.

Assuming that the voltage across $L_{S(HV)}$ remains negligible, this directly causes a corresponding linear rise in voltage across $R_{G(HV)}$ throughout this period, since $V_{GS(HV)}$ remains clamped at $V_{T(HV)}$. This leads to a linear increase in Miller current, a linear increase in $\frac{dV_{DS(casc)}}{dt}$.



The continually-increasing Miller current in this period has a significant impact on $I_{S(HV)}$. Since $I_{D(casc)}$ remains clamped at I_L throughout this period, the HV Miller current directly reduces the HV source current and hence also reduces $I_{S(HV)}$, since $I_{S(HV)} = I_L - C_{DG(HV)} \frac{dV_{DS(HV)}}{dt}$. This effect both reduces the turn-off losses in the LV switch and allows $I_{D(casc)}$ to fall faster in the following stage, since the current in $L_{S(HV)}$ at the beginning of stage IX is somewhat lower than I_L .

Provided the internal gate resistance is known, this effect can easily be corrected for in such measurements and a good fit found with this idealised model. Some care is still required, however: In the case of the SiC JFET discussed previously, the voltage drop across the internal gate resistance can be sufficient to cause reverse breakdown of the gate-source diode. It is therefore important to ensure that gate ratings are not exceeded during this stage of switching.

4.9.2.3 Stage IX ($\tau_I \leq t < \tau_J$) - Drain current falls

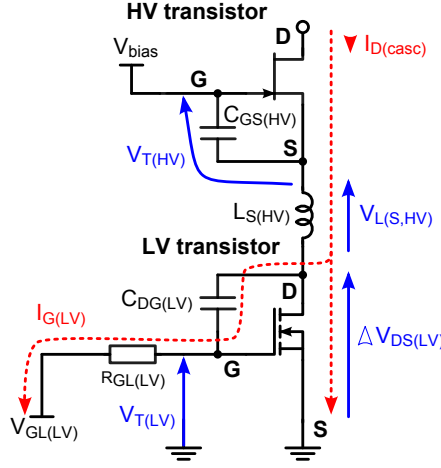


Figure 4.27: Equivalent circuit for stage IX

$V_{DS(casc)}$ reaches V_{DC} at τ_I , resulting in an abrupt end to the Miller current in the HV gate circuit, causing V_G to fall rapidly to V_{bias} . $V_{GS(HV)}$ remains clamped at approximately $V_{T(HV)}$ whilst $I_{D(casc)} > 0$, so there is a corresponding rapid fall in voltage at the source of the HV transistor to $V_{bias} - V_{T(HV)}$.

A voltage difference of $V_{DS(LV)} - V_{bias} + V_{GS(HV)}$ is therefore imposed across $L_{S(HV)}$ causing current to fall. However, since the current flowing in $L_{S(HV)}$ at the beginning of this period is already lower than I_L , having been able to fall during the previous stage, a step-change drop in $I_{D(casc)}$ is observed at τ_I .

The precise behaviour of $V_{DS(LV)}$ during this period is complex, since it is dependent on both feedback in gate circuit of the LV transistor and $L_{S(HV)}$ as described by the differential equation:

$$L_{S(HV)}g_{m(LV)}R_{GL(LV)}C_{DG(LV)}\frac{d^2V_{DS(LV)}}{dt^2} + V_{DS(LV)} - V_{bias} + V_{T(HV)} = 0 \quad (4.6)$$

The solution for this in terms of $V_{DS(LV)}$ has the form:

$$V_{DS(LV)} = A \sin(Dt) + B \cos(Dt) + C \quad (4.7)$$

Where:

$$D = \sqrt{\frac{1}{L_{S(HV)}(C_{DG(LV)} + g_{m(LV)}R_{GL(LV)}C_{DG(HV)})}} \quad (4.8)$$

As the inductor voltage falls to zero, the voltages at the source of the HV switch and the drain of the LV switch rapidly equalise, causing charge to be transferred from C_{oss} into the HV gate circuit, consisting of $R_{G(HV)}$ and $C_{GS(HV)}$. Some of the energy transferred from $C_{oss(LV)}$ is dissipated in $R_{G(HV)}$, which sees an exponential decrease in the voltage across it. This energy dissipation may be written as:

$$E_{diss,R_{G(HV)}} = \frac{V_{initial}^2}{R_{G(HV)}} \int_0^\infty e^{-\frac{2t}{R_{G(HV)}C_{GS(HV)}}} = \frac{1}{2}C_{GS(HV)}V_{initial}^2 \quad (4.10)$$

Where $V_{initial} = V_{bias} - \hat{V}_{DS(LV)} - V_{T(HV)}$

The energy in the two capacitances following this voltage equalisation process is easily calculated based on the final voltage across each. This leads to an expression for the total energy at the end of this process of:

$$E_{final} = \frac{1}{2} \left[C_{oss(LV)}V_{DS(LV,off)}^2 + C_{GS(HV)}(V_{bias} - V_{DS(LV,off)})^2 + C_{GS(HV)}V_{initial}^2 \right] \quad (4.11)$$

Where $V_{DS(LV,off)}$ is the voltage across the LV transistor at the end of the period.

The final voltage across the LV transistor may therefore be calculated by equating the initial and final energies of this process. The quadratic nature of this expression is not convenient. However, in the case of the JFET, where $V_{bias} \ll V_{DS(LV,off)}$, this may be approximated as:

$$V_{DS(LV,off)} \approx \sqrt{\frac{C_{oss(LV)}\hat{V}_{DS(LV)}^2 + C_{GS(HV)}(V_{T(HV)}^2 - (V_{bias} - \hat{V}_{DS(LV)} - V_{T(HV)})^2)}{C_{oss(LV)} + C_{GS(HV)}}} \quad (4.12)$$

In the case of enhancement mode devices such as the SiC MOSFET where V_{bias} is large and of similar magnitude to $V_{DS(LV,off)}$, this may be approximated as:

$$V_{DS(LV,off)} \approx \sqrt{\frac{C_{oss(LV)}\hat{V}_{DS(LV)}^2 + C_{GS(HV)}V_{T(HV)}^2}{C_{oss(LV)} + C_{GS(HV)}}} \quad (4.13)$$

4.10 Validating the idealised switching model

The system of equations of the simplified cascode switching model are presented in table 4.5. Switching traces for a 600 V, 25 A clamped inductive load calculated using these simplified equations are compared against experimental measurements in figure 4.18.

Period	$V_{DS(casc)}$	$I_D(casc)$	$V_{DS(LV)}$	$V_{GS(LV)}$	$V_{G(HV)}$	$V_{GS(HV)}$	$I_{S(HV)}$
Stage I	V_{DC}	0	$\approx V_{DS(LV,off)}$	$(V_{GH(LV)} - V_{GL(LV)})(1 - e^{-\frac{\tau_{eqA}}{R_{GH(LV)}C_{GS}}}) + V_{GL(LV)}$	V_{bias}	$\frac{V_{bias} - V_{DS(LV,off)}}{V_{DS(LV,off)} + k_{on}(t - \tau_B)}$	0
Stage II			$V_{DS(LV,off)} - k_{on}(t - \tau_B)$	$V_{T(LV)}$	$V_{bias} - V_{DS(LV,off)} + k_{on}(t - \tau_B)$	$V_{T(HV)}$	
Stage III			$\frac{V_{bias} - V_{T(HV)}}{L_{S(HV)}}(t - \tau_C)$				
Stage IV	$V_{DC} - \frac{V_{bias} - V_{T(HV)}}{R_{G(HV)}C_{DG(HV)}}(t - \tau_D)$	I_L	0	$(V_{GH(LV)} - V_{T(LV)})(1 - e^{-\frac{t - \tau_C}{R_{GH(LV)}C_{GS}}}) + V_{T(LV)}$	$V_{T(HV)}$	$V_{T(HV)}$	$I_L + \frac{V_{bias} - V_{T(HV)}}{R_{G(HV)}}$
Stage V	0				$V_{T(HV)}$	V_{bias}	I_L

(a) Turn-on

Period	$V_{DS(casc)}$	$I_D(casc)$	$V_{DS(LV)}$	$V_{GS(LV)}$	$V_{G(HV)}$	$V_{GS(HV)}$	$I_{S(HV)}$
Stage VI	0	I_L	0	$(V_{GH(LV)} - V_{GL(LV)})e^{-\frac{(t - \tau_D)}{R_{GL(LV)}C_{GS(LV)}}} + V_{GL(LV)}$	V_{bias}	$\frac{V_{bias}}{V_{bias} - k_{off}(t - \tau_G)}$	I_L
Stage VII	0			$V_{T(LV)}$	$V_{bias} + k_{off}(t - \tau_H)$	$V_{T(HV)}$	$I_L - \frac{k_{off}(t - \tau_H)}{R_{G(HV)}}$
Stage VIII	$\approx \frac{k_{off}(t - \tau_H)^2}{2C_{DG(HV)}R_{G(HV)}}$			$\approx V_{T(LV)}$	V_{bias}	$V_{T(HV)}$	$I_D(casc)$
Stage IX	V_{DC}	$I_L - \frac{k_{off}(t - \tau_G)}{R_{G(HV)}} - \frac{k_{off}(t - \tau_G) - V_{bias} + V_{T(HV)}}{L_{S(HV)}}(t - \tau_I)$	$V_{DS(LV,off)}$	$(V_{T(LV)} - V_{GL(LV)})e^{-\frac{(t - \tau_D)}{R_{GL(LV)}C_{GS(LV)}}} + V_{GL(LV)}$	V_{bias}	$V_{bias} - V_{DS(LV,off)}$	$I_D(casc)$
Stage X		0					

(b) Turn-off

Where $k_{on} = \frac{V_{GH(LV)} - V_{T(LV)}}{R_{GH(LV)}C_{DG(LV)}}$, $k_{off} = \frac{V_{T(LV)} - V_{GL(LV)}}{R_{GL(LV)}C_{DG(LV)}}$,

$$V_{DS(LV,off)} \approx \begin{cases} \sqrt{\frac{C_{oss(LV)} \hat{V}_{DS(LV)}^2 + C_{GS(HV)} (V_{T(HV)}^2 - (V_{bias} - \hat{V}_{DS(LV)} - V_{T(HV)})^2)}{C_{oss(LV)} + C_{GS(HV)}}} & V_{bias} \ll V_{DS(LV,off)} \\ \sqrt{\frac{C_{oss(LV)} \hat{V}_{DS(LV)}^2 + C_{GS(HV)} V_{T(HV)}^2}{C_{oss(LV)} + C_{GS(HV)}}} & V_{bias} \approx V_{DS(LV,off)} \end{cases}$$

Table 4.5: Summary of equations derived for simplified cascode switching model

Parameter	Value	Parameter	Value
$L_{S(HV)}$	7.5 nH	$V_{T(LV)}$	2.5 V
$R_{GL(LV)}$	6.94 Ω	$V_{T(HV)}$	-4.5 V
$R_{GH(LV)}$	4.20 Ω	$C_{DG(LV)}$	500 pF
$R_{GH(HV)}$	6 Ω	$C_{GS(LV)}$	5.5 nF
V_{DC}	600 V	$C_{DS(LV)}$	1 nF
I_L	25 A	$C_{DG(HV)}$	70 pF
V_{bias}	2.5 V	$C_{GS(HV)}$	175 pF
$V_{GH(LV)}$	10 V	$C_{DS(HV)}$	0 pF
$V_{GL(LV)}$	0 V		

Table 4.6: List of model parameter values used in simplified model of figure 4.18

4.10.1 Selection of model variable values

The model parameters used in these calculations are given in table 4.6. The gate resistances used include both device internal gate resistance and gate driver resistance in addition to discrete external resistances. The parasitic capacitance values used are for $V_{DS(LV)} = 2$ V for the LV device and for $V_{DS(HV)} = 300$ V for the HV device.

The initial values of $V_{DS(LV)}$ and $V_{GS(HV)}$ at turn-on are calculated by first running the model to determine their final value at the end of turn-off and setting this as the initial condition. It should be noted that the modelled $V_{G(HV)}$ waveform has been scaled to allow direct comparison with the experimental measurements, by accounting for the fact that internal resistance of the HV JFET acts to form a potential divider with $R_{G(HV)}$. The actual value of $V_{G(HV)}$ predicted by the simplified equations has a value of:

$$V_{G(HV,actual)} = \frac{R_{G(HV)} + R_{G(HV,int)}}{R_{G(HV)}} (V_{G(HV,given)} - V_{bias}) + V_{bias} = 6(V_{G(HV,given)} - 2.5) + 2.5 \quad (4.14)$$

4.10.2 Comparison between idealised model and experimental measurements

The simplified model in general shows good agreement with the experimental measurements, although some experimentally measured effects are clearly not modelled.

Both cascode drain voltage and current waveforms show a reasonable match to the experimental traces, although the simplified model tends to underestimate $\frac{dV_{DS(cascode)}}{dt}$ at high voltages, as explained in section 4.10.3.

The $V_{DS(LV)}$ trace shows some of the limitations of the assumption of constant capacitance and underestimates $\frac{dV_{DS(HV)}}{dt}$ at higher voltages. However, the model does successfully capture both the peak and final values of $V_{DS(LV)}$. The accuracy of estimating these values is aided by the dependence of the rise-time of $V_{DS(casc)}$ on $\frac{dV_{DS(LV)}}{dt}$. Any underestimate of $\frac{dV_{DS(LV)}}{dt}$ in the model is counteracted by a longer rise-time of $V_{DS(casc)}$ and vice-versa. The close match between the simplified model and measurement in Stage X indicates that the charge redistribution mechanism described by equation 4.12 is a good description of the process.

Discrepancies between experimental measurements of $V_{GS(HV)}$ and the predictions of the the simplified model may largely be explained by the difficulties of measuring $V_{GS(HV)}$ experimentally, as previously discussed in section 4.6.1.3. Indeed there is a good match between the ‘ideal’ measurements of $V_{GS(HV)}$ from the SPICE model in figure 4.16 and those of the simplified analytical model in figure 4.18.

The simplified model does not take account of the significant noise in the measurements at $V_{G(HV)}$. Some of this noise is spurious measurement interference, whilst some is related to parasitic oscillations. The majority of this noise has little overall effect on the switching behaviour of the cascode. Therefore, whilst the voltage and current noise at this location is not accurately modelled, the overall effect of $V_{G(HV)}$ on the behaviour of the cascode matches well with experiment. However, the simplified model is unsuitable for predicting EMI behaviour.

There is a slight anomaly in the prediction of $V_{GS(LV)}$ by the simplified model, with its rise time predicted to be slightly slower than measurement and its fall time faster than measurement. This is likely to be an effect of the value selected for C_{iss} . The datasheet values on which the value was based assume a V_{GS} of 0 V. In reality, there usually a positive relationship between V_{GS} and C_{iss} , which is not accounted for in the model [187].

4.10.3 Capacitance value selection

Due to the assumption of constant device capacitance, the simplified model is sensitive to the selection of parasitic capacitance values for both transistors. Since V_{DS} changes during switching, capacitor value selection is a trade-off between over-estimating $\frac{dV_{DS}}{dt}$ at low V_{DS} and under-estimating it at high V_{DS} .

For the purposes of device selection, this limitation is not a great problem. For most transistors, capacitance changes monotonically with V_{DS} . For devices of similar voltage and current ratings, this means that a transistor with significantly higher parasitic capacitance than another at one voltage is likely to have a significantly higher parasitic capacitance over the entire range of V_{DS} . In contrast, devices with only small differences in parasitic capacitance are likely to have similar switching characteristics anyway, all other parameters being equal.

Provided the parasitic capacitance values used are all extracted under similar conditions (i.e. identical V_{DS}), the simplified model will give a good indication of the comparative benefits of the different devices.

4.10.4 Design equations

The expressions described in table 4.5 can be rearranged into a series of design equations to estimate a range of switching parameters. The equations for peak parameter values are found by substituting the time taken to reach that value into the the relevant switching model equations. The switching loss equations are calculated as:

$$E_{loss(on)} = \int_{\tau_c}^{\tau_E} V_{DS(casc)} I_{D(casc)} dt$$

and

$$E_{loss(off)} = \int_{\tau_G}^{\tau_f} V_{DS(casc)} I_{D(casc)} dt$$

using the equations for $V_{DS(casc)}$ and $I_{D(casc)}$ given in table 4.5

The design equations are listed in table 4.7.

4.11 Implications of the simplified model

4.11.1 Controlling transients

A feature of cascode switches is their ability to produce high $\frac{dV}{dt}$ and $\frac{dI}{dt}$. This is advantageous for reducing switching losses, but may cause excessive electromagnetic interference. Based on the equations in table 4.7, switching $\frac{dV}{dt}$ can only be significantly limited by increasing $R_{G(HV)}$ or $C_{DG(HV)}$, although turn-off $\frac{dv}{dt}$ can also be limited by increasing $R_{GL(LV)}$. Increasing $R_{G(HV)}$ may increase susceptibility to spurious turn-on and will increase peak $V_{DS(LV)}$. Hence, control of $\frac{dV}{dt}$ is best effected by increasing $C_{DG(HV)}$, confirming the findings of Aggeler et. al. [142].

Control of $\frac{dI}{dt}$ is beyond the direct control of either gate circuit. Limited control is achievable at turn-off by increasing $C_{DG(HV)}$, $C_{DG(LV)}$ or $R_{GL(LV)}$, although $\frac{dV}{dt}$ and switching losses are also affected. Turn-on $\frac{dI}{dt}$ may be controlled by altering the DC gate bias of the HV device, raising the interesting possibility of a cascode with an active HV gate drive. In some cases $\frac{dI}{dt}$ could perhaps be tailored by laying out the cascode circuit to have a specific value of $L_{S(HV)}$.

Parameter	Turn on	Turn off
Peak $\frac{dI}{dt}$	$\frac{V_{bias}-V_{T(HV)}}{L_{S(HV)}}$	$-\frac{V_{rise}}{L_{S(HV)}}$
Peak $\frac{dV}{dt}$	$-\frac{V_{bias}-V_{T(HV)}}{R_{G(HV)}C_{DG(HV)}}$	$\sqrt{\frac{2V_{DC}k_{off}}{R_{G(HV)}C_{DG(HV)}}}$
Turn-on loss	$\frac{I_L V_{DC}}{2} \left(\frac{I_L L_{S(HV)}}{V_{bias}-V_{T(HV)}} + \frac{V_{DC} R_{G(HV)} C_{DG(HV)}}{V_{bias}-V_{T(HV)}} \right)$	
Turn-off loss	$V_{DC} \left(\frac{I_L}{3} \sqrt{\frac{2V_{DC} R_{DG(HV)} C_{DG(HV)}}{k_{off}}} + \frac{I_0^2 L_{S(HV)}}{2V_{rise}} \right)$	
Peak $V_{DS(LV)}$	$V_{bias} - V_{T(HV)} + V_{rise}$	
Peak $V_{GS(HV)}$	$V_{bias} - V_{DS(LV,off)}$	

Where:

$$k_{off} = \frac{V_{T(LV)} - V_{GL(LV)}}{R_{GL(LV)} C_{DG(LV)}}, V_{rise} = \sqrt{2V_{DC} R_{G(HV)} C_{DG(HV)} k_{off}}, I_0 = I_L - \sqrt{\frac{2k_{off} C_{DG(HV)} V_{DC}}{R_{G(HV)}}} \text{ and}$$

$$V_{DS(LV,off)} \approx \begin{cases} \sqrt{\frac{C_{oss(LV)} \hat{V}_{DS(LV)}^2 + C_{GS(HV)} (V_{T(HV)}^2 - (V_{bias} - \hat{V}_{DS(LV)} - V_{T(HV)})^2)}{C_{oss(LV)} + C_{GS(HV)}}} & V_{bias} \ll V_{DS(LV,off)} \\ \sqrt{\frac{C_{oss(LV)} \hat{V}_{DS(LV)}^2 + C_{GS(HV)} V_{T(HV)}^2}{C_{oss(LV)} + C_{GS(HV)}}} & V_{bias} \approx V_{DS(LV,off)} \end{cases}$$

Table 4.7: Equations to describe key performance parameters

4.11.2 Peak $V_{DS(LV)}$

The peak voltage across the LV device must be limited to avoid damage to the device, parasitic ringing at turn-off and excessive negative $V_{GS(HV)}$. By rearranging the equation for $\hat{V}_{DS(LV)}$, an expression may be derived to estimate the minimum turn-off gate resistance required for a given maximum $V_{DS(LV)}$ (V_{pk}):

$$R_{min} = \frac{2R_{G(HV)} C_{DG(HV)} V_{DC}}{(V_{pk} - V_{bias} + V_{T(HV)})^2 C_{DG(LV)}} \quad (4.15)$$

A good choice for V_{pk} is halfway between the rated breakdown voltage of the HV gate-source junction and $V_{T(HV)}$.

4.11.3 Noise immunity

A positive $\frac{dV_{DS(casc)}}{dt}$, causes an increase in $V_{DS(LV)}$ and $V_{GS(LV)}$, with the reverse happening for a negative $\frac{dV_{DS(casc)}}{dt}$. However, the effect on $V_{GS(HV)}$ depends on the relative values of device parasitics and can either increase or decrease due to a voltage transient.

Noise immunity could be improved by ensuring that $C_{GS(HV)}$ is much greater than $C_{DG(HV)}$ or $C_{DS(HV)}$ to ensure the majority of a transient is shunted to ground via the HV gate circuit. Increasing $C_{GS(HV)}$ has little effect on switching speeds. Ensuring that $C_{oss(LV)}$ is significantly greater than $C_{oss(HV)}$ would help to limit the transients experienced by the LV switch and $C_{oss(LV)}$ can be comparatively large without significantly impacting switching losses.

4.11.4 Switching delays

The need to use small turn-on and large turn-off resistors [185] for effective cascode gate drive leads to asymmetric delays. This behaviour must be accounted for in applications such as bridge circuits, where the differences in delay times must be dealt with either by adjusting the gate drive signals to each device or by extending the dead time.

4.11.5 Ideal device selection

For a fast switching cascode with maximum noise immunity, a low-inductance HV device with very small C_{oss} and C_{rss} and a proportionally large C_{iss} is desirable. A reasonably large $V_{T(HV)}$ will aid turn-on speed and a large negative gate-source breakdown voltage will benefit transient immunity. The LV device should have a voltage rating comfortably exceeding the maximum anticipated V_{DS} , comparatively large C_{oss} , C_{iss} and V_T , but small stray inductance, C_{rss} and on-state resistance.

4.11.6 Off-state leakage currents

The simplified model does not consider the possibility of leakage currents through the channel of either device in the off-state. Such leakage current will cause $V_{DS(LV)}$ and hence also $V_{GS(HV)}$ to drift if the cascode is required to block voltage continuously for an extended period. This effect is self-limiting if it causes $V_{DS(LV)}$ to fall. However, rising $V_{DS(LV)}$ due to leakage currents will eventually cause drain-source breakdown of the LV transistor or gate-source breakdown of the HV device.

4.11.7 Conclusions

Despite some discrepancies with measured values, the behaviour predicted by the simplified model gives a good first-order description of the behaviour of the cascode circuit. Modelling accuracy could be improved by including the effects of voltage-dependent capacitances and device internal resistance. However, this is unnecessary for simple device comparisons.

The simplicity of the derived equations makes it possible to produce a series of design equations for aiding cascode design. Using these equations, the conclusions of other authors have been validated.

4.12 Cascode modelling conclusions

The modelling and analysis presented in this chapter have described the cascode switching process in detail and produced two useful models of cascode switching that inform the rest of this thesis.

The SiC JFET SPICE model has shown that it is possible to generate an effective simulation model of a SiC vertical power JFET without resorting to complex equivalent circuits or carrier-level simulations. The hybrid cascode model it is part of has been validated by comparison with experimental measurements and will be used in following chapters to complement experimental work.

The idealised model of cascode switching developed in this chapter has also been shown to be capable of predicting cascode switching behaviour with reasonable accuracy. Despite its simplicity, it is capable of providing a clear insight into the dynamic behaviour of cascode circuits and corroborating the findings of other authors.

The findings of both models will be used in conjunction with the experimental findings of the following two chapters to produce a cascode design guide as part of the conclusion of this thesis in chapter 7.

Chapter 5

Static characterisation

5.1 Introduction

Static characterisation of semiconductor devices is important for establishing their forward conduction, reverse conduction and breakdown behaviour. This allows forward and reverse conduction losses as well as device operating limits to be estimated. When combined with switching loss measurements, good estimates of device performance in specific applications can be calculated.

In this chapter, the steady-state behaviour of two HV SiC transistors is compared with that of a conventional HV Si super-junction (SJ) MOSFET. The static characteristics of these three individual devices are then compared with those of the same devices when operated in a cascode configuration. For each device combination, the current-voltage (I-V) and transfer characteristics (I_D vs V_{GS}) are examined and the differences in $R_{DS(ON)}$, V_T and g_m are explained. The possibility of using cascode reverse conduction as a free-wheel path and the high temperature behaviour of the two HV SiC devices are also investigated.

5.2 Device selection

Three commercial HV FETs were chosen for comparison. These were: a silicon super-junction MOSFET, a silicon carbide MOSFET, and a SiC JFET. All the devices were targeted at similar power conversion applications and were marketed on the strength of their low $R_{DS(ON)}$ and high blocking voltage. The Si SJ MOSFET is promoted on the basis of its simple drive requirements and fast body diode [188]; the SiC MOSFET emphasises its high switching speed due to its low capacitances [145]; whilst the SiC JFET advertises its exceptionally low gate charge and ease of paralleling [79].

IGBTs were excluded from the comparison, since their inherently long switching delays and tail current are likely to both eliminate any benefits of cascode operation.

5.2.1 Silicon carbide devices

The SiC JFET and MOSFET used were commercially available 1200 V devices with similar current and $R_{DS(ON)}$ ratings. This provided an attractive basis for comparison. Their identical TO-247 packages minimised differences in layout that might affect their dynamic characteristics, studied in chapter 6.

The SiC devices used were the Semisouth SJDP120R085 SiC vertical JFET and the Cree C2M0080120D SiC MOSFET. These had current ratings at 25 °C of 27 A and 36 A respectively and an $R_{DS(ON,max)}$ of 85 m Ω and 98 m Ω respectively.

The Semisouth SJDP120R085 is now an old device and its manufacturer no longer exists. However, new SiC JFETs are becoming available from suppliers such as United SiC [189]. The Semisouth devices have broadly similar characteristics to the United SiC devices [79, 189] and apparently slightly better characteristics in several areas, including lower C_{DG} , C_{iss} and lower leakage current. For this reason, the Semisouth device is still representative of SiC JFET technology.

SiC BJTs with similar ratings have become available since this work was carried out. These devices may also benefit from use in a cascode configuration, although this has not been investigated to date.

5.2.2 Silicon devices

To compare SiC and silicon transistors, devices with similar current ratings and $R_{DS(ON)}$ are required. This presents a difficulty: Simple Si MOSFETs are unable to withstand the high blocking voltages under investigation without excessive $R_{DS(ON)}$. However, the emergence of SJ MOSFETs has made devices capable of blocking large voltages at a much lower $R_{DS(ON)}$ a reality and these will be considered here.

Although SJ devices with blocking voltages up to 900 V exist, none have an $R_{DS(ON,max)}$ below 120 m Ω , so were not considered to be a good match for the SiC devices. Instead, the 650 V rated, 43.3A IPW65R080CFD in a TO-247 package with an $R_{DS(ON,max)}$ of 80 m Ω was chosen. This enables a direct comparison between Si and SiC devices to be made, albeit at significantly below the rated voltage of the SiC devices.

It is important that this difference in voltage rating is taken into account when comparing performance; in general, higher voltage parts tend to suffer from higher $R_{DS(ON,max)}$ and can also have larger C_{iss} and C_{oss} , affecting both on-state and switching performance. Although it

would perhaps be preferable to compare the 650 V Si SJ MOSFET with 650 V SiC devices, no devices with comparable electrical characteristics were available, which would have made direct comparison between devices particularly difficult.

In addition to the HV devices, a LV Si MOSFET was required for cascode operation. The 60 V, 49 A Fairchild FDMS5352 was chosen for this purpose for its small $R_{DS(ON,max)}$ of 6.7 m Ω , reasonably high $V_{DS(max)}$ and low inductance PQFN package. This ensured that it could cope with potentially large voltage spikes due to the cascode circuit, whilst minimising its contribution to on-state $R_{DS(ON)}$ and avoiding unnecessarily adding parasitic inductance to the cascode circuit. The properties of the transistors used are summarised in table 5.1.

Device	IPW65R080CFD	C2M0080120D	SJDP120R085	FDMS5352
Type	Si SJ MOSFET	SiC MOSFET	SiC JFET	Si MOSFET
$V_{DS(max)}$	650 V	1200 V	1200 V	60 V
$I_{D(max)}$	43.3 A	36 A	27 A	49 A
$\hat{R}_{DS(ON)}$	80 m Ω	85 m Ω	98 m Ω	6.7 m Ω
$C_{iss(typ)}$	5030 pF	950 pF	255 pF	5220 pF
$C_{oss(typ)}$	70 pF	82 pF	0 pF	410 pF
$C_{rss(typ)}$	25 pF	7.6 pF	35 pF	255 pF
$T_{J(max)}$	150 °C	150 °C	150 °C	150 °C
$V_{T(typ)}$	4.0 V	3.0 V	-5.0 V	1.8 V

Table 5.1: Properties of transistors used. All measurements are at 25 °C. HV capacitance measured at $V_{DS} = 600$ V, LV capacitance measured at $V_{DS} = 30$ V [79, 145, 171, 188]

5.3 I-V Characteristics

The I-V characteristics of each HV device combination were measured for both forward and reverse conduction using a curve tracer (see chapter 3). A similar set of measurements was then taken for each HV device in a cascode arrangement with the LV Si MOSFET. Although I-V characteristics for the individual transistors are provided in their datasheets, it is easier to directly compare the I-V characteristics of all device combinations when they are measured under identical conditions.

Measurements were taken at a room temperature of 21 °C \pm 1 °C, with the device mounted on a heatsink to ensure a consistent operating temperature. Forward and reverse conduction behaviour is considered separately below:

5.3.1 Standalone devices

I-V curves for each individual device are shown in figure 5.1.

5.3.1.1 Forward conduction (first quadrant of I-V curve)

The forward conduction I-V characteristics of the HV devices are superficially similar. The gradient of the curves maximum V_{GS} are similar for each, due to the matched $R_{DS(ON)}$ characteristics of the devices. However, there is substantial variation between both the threshold voltages (V_T) and the forward transconductances (g_m) of the devices, apparent as the very different values of V_{GS} required to achieve a given operating point.

Mobility effects The difference in V_T is unsurprising, particularly as the SiC JFET is a depletion mode device. The variation in g_m is more interesting and is due to different device mobilities. SiC has a carrier mobility approximately 50% lower than that of silicon [38] and SiC MOSFETs have even lower channel mobility still. Carrier mobility directly impacts the transconductance of transistors. For a device operation in the saturation region, the transconductance, g_m may be expressed using the Shichman–Hodges MOSFET model as [174]:

$$g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

Hence there is an approximately linear relationship between mobility and transconductance. This explains why g_m for the SiC JFET is lower than that of the Si SJ MOSFET and why the SiC MOSFET has a lower g_m than either of the other devices. As a result, a very large change in V_{GS} is required to fully enhance the SiC MOSFET in comparison to the other devices, which explains its high voltage drive requirements.

In general, this means that the gate drive requirements for the SiC devices are likely to be more onerous than those of Si devices. The SiC MOSFET requires at least double the gate drive voltage to approach full channel enhancement, whilst the SiC JFET ideally requires a gate driver capable of both positive and negative drive voltages. These are not severe difficulties, but do add to the cost and complexity of gate driver circuits.

A further comparison of g_m and $R_{DS(ON)}$ between the individual and cascode devices is made in sections 5.3.3 and 5.3.4.

Short-channel effects Short-channel effects, as described in section 4.4.4, are visible in the forward I-V curves for both SiC devices. Compared to the Si SJ MOSFET, the curves are less flat and tend to level off more slowly in the saturation region. This is due to the channel length

of the SiC devices being of a similar magnitude to the depletion widths at the drain and the source [176].

An effect of this that is particularly noticeable here is channel length modulation, which occurs when the drain voltage exerts undue influence on the channel and allows increasing current to flow at greater drain bias. This leads to the characteristic sloping effect apparent in figure 5.1, where there is a strong dependence of I_D on V_{DS} in the saturation region, particularly at larger V_{GS} [64, 176].

Short-channel effects are not severely detrimental to the performance of switching devices, but they must be accounted for if they are to be accurately modelled.

LV Si MOSFET In contrast to the HV devices, the LV MOSFET shows very high g_m and very low $R_{DS(ON)}$. Being a low voltage device, it comes somewhat closer to the ‘ideal’ MOSFET of the Shichman-Hodges model.

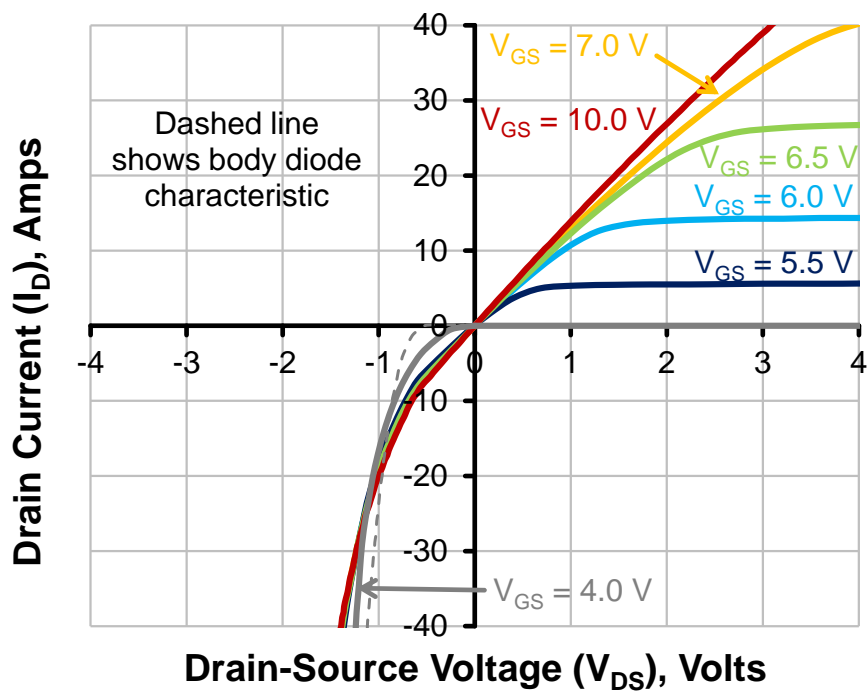
5.3.1.2 Reverse conduction (third quadrant of I-V curve)

The behaviour of the four transistors is markedly different under reverse conduction conditions:

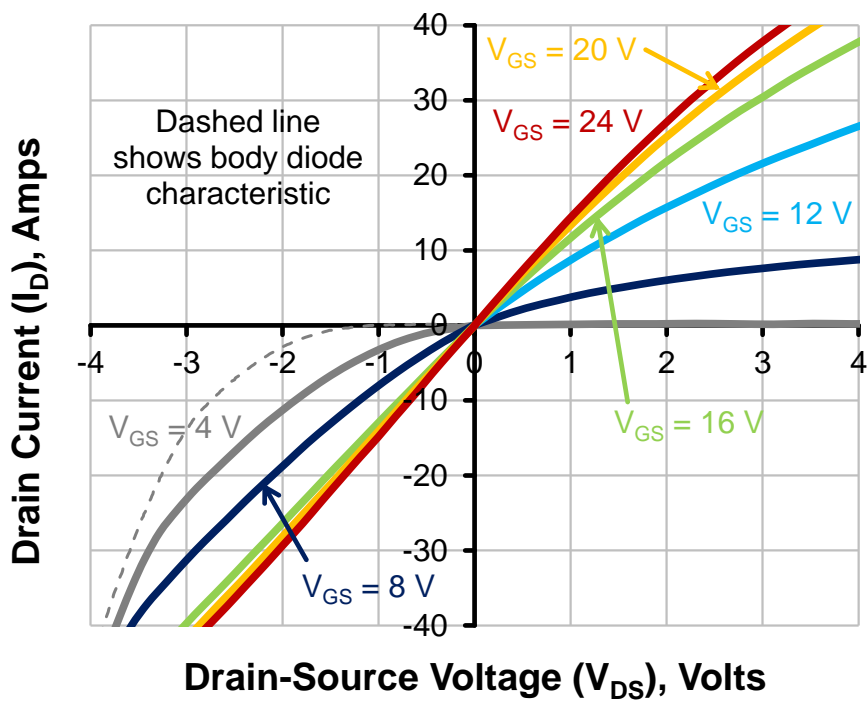
Si SJ MOSFET The very low forward voltage (V_f) of around 0.6 V of the Si SJ MOSFET body diode is particularly apparent. Reverse conduction takes place entirely in the channel until the body diode is forward biased, after which the majority of drain current is carried by the diode. This point is visible in figure 5.1a as the kink in the reverse characteristics. For reverse currents over a few amps, forward biasing the body diode is unavoidable, even if the channel is fully enhanced.

It is interesting to note that at higher currents, $|V_{DS}|$ actually becomes larger when both the current is shared between channel and body diode, compared to the body diode conducting the current alone. This is likely to be due to carriers in the channel in its on-state interfering with the equilibrium of the body diode and resulting in a flatter body diode characteristic [190].

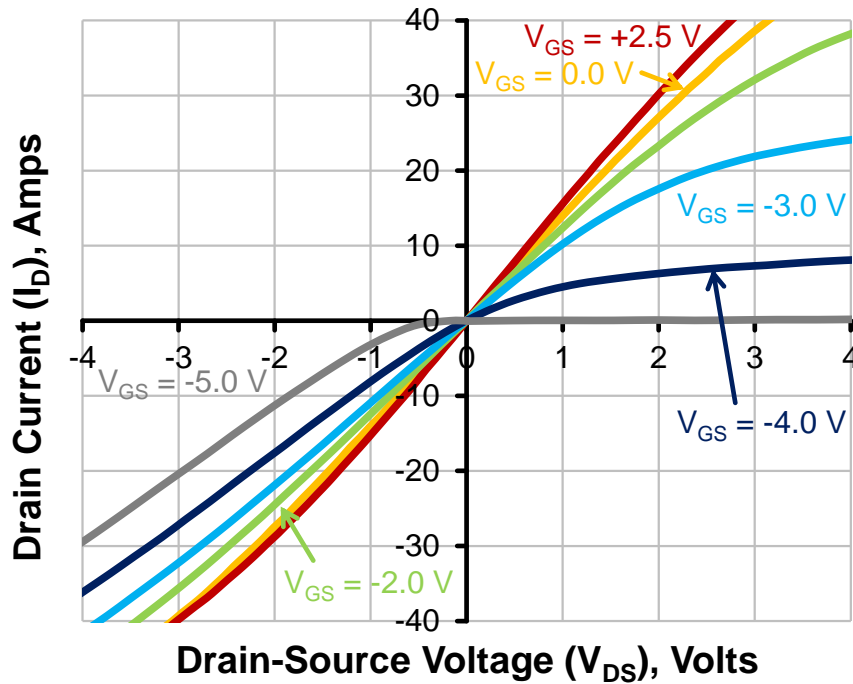
SiC MOSFET The SiC MOSFET reverse characteristic has similarities with that of the SJ MOSFET. However, the P-N body diode starts conducting only at around 1.5 V and has a much smoother transition from blocking to conducting, due to the much wider bandgap of SiC. As can be seen in the trace for $V_{GS} = 4$ V, any positive V_{GS} will bring reduce the onset of reverse conduction from V_f , even if it is less than V_T . This is because a MOSFET, like all FETs is an approximately symmetrical device and therefore its channel will start conducting once $V_{GD} = V_{GS} - V_{DS} > V_T$.



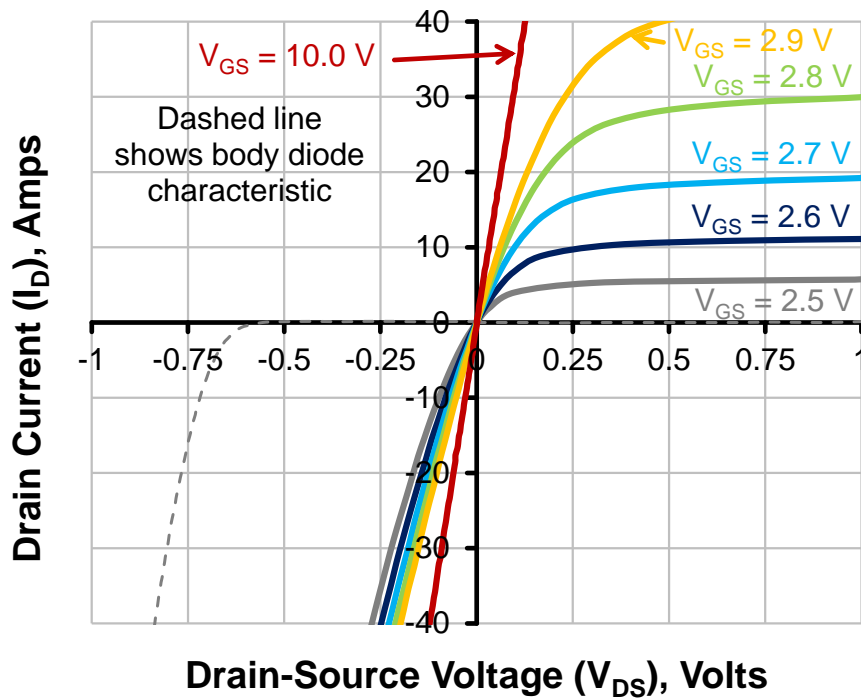
(a) Si SJ MOSFET



(b) SiC MOSFET



(c) SiC JFET



(d) LV Si MOSFET

Figure 5.1: I-V curves for individual devices in forward and reverse conduction (Note different horizontal axis for LV device)

In general, reverse conduction in the SiC MOSFET will always forward bias the body diode at currents above approximately 20 A. However, even at rated current, body diode current accounts for only around 10 % of the total drain current if the channel is fully enhanced.

SiC JFET The SiC JFET is notable for its obvious lack of a body diode. This is thanks to its vertical structure which ensures no drain-source P-N junctions exist. However, reverse conduction is still inevitable, albeit by a slightly different mechanism. As with the SiC MOSFET, the JFET will conduct once $V_{GD} = V_{GS} - V_{DS} > V_T$. Therefore, reducing the gate voltage simply increases the magnitude of V_{DS} at which reverse conduction commences. Since V_{GS} can never exceed around -15 V without risking damage to the gate, reverse conduction is unavoidable for $V_{DS} < V_T - 15$.

If the channel is fully enhanced, the SiC JFET has similar reverse I-V characteristics to the SiC MOSFET, with the advantage that, with no P-N junction to forward bias, there can be no issue of carrier lifetime to cause problems with reverse recovery.

LV Si MOSFET In contrast to the HV devices, the LV Si MOSFET has such low $R_{DS(ON)}$ that when the channel is fully enhanced, the body diode is never forward biased, even at its rated current. Hence this device could be used in the on-state under reverse bias with no reverse recovery issues.

5.3.2 Cascode

I-V curves for the HV devices in a cascode configuration with the LV Si MOSFET device are shown in figure 5.3.

5.3.2.1 Forward conduction (first quadrant of I-V curve)

Characteristic behaviour In the cascode configuration, the forward conduction characteristics for all three circuits are almost identical. This is because of the unique behaviour of the cascode circuit: The LV switch initially blocks the entire voltage. Rising $V_{DS(LV)}$ causes $V_{GS(HV)}$ to fall until it reaches $V_{T(HV)}$. As soon as the HV switch begins to switch off, it blocks any further increases in $V_{DS(casc)}$, causing $V_{DS(LV)}$ to abruptly plateau, even though $V_{DS(casc)}$ continues to rise.

This leads to an interesting composite forward I-V characteristic, in which the gradient of the linear region is determined by the $R_{DS(ON)}$ of the HV device, whilst the saturation region is determined by the characteristics of the LV device, albeit to a much higher voltage. However, the cascode I-V curve only follows the LV I-V curve until the point where the HV transistor

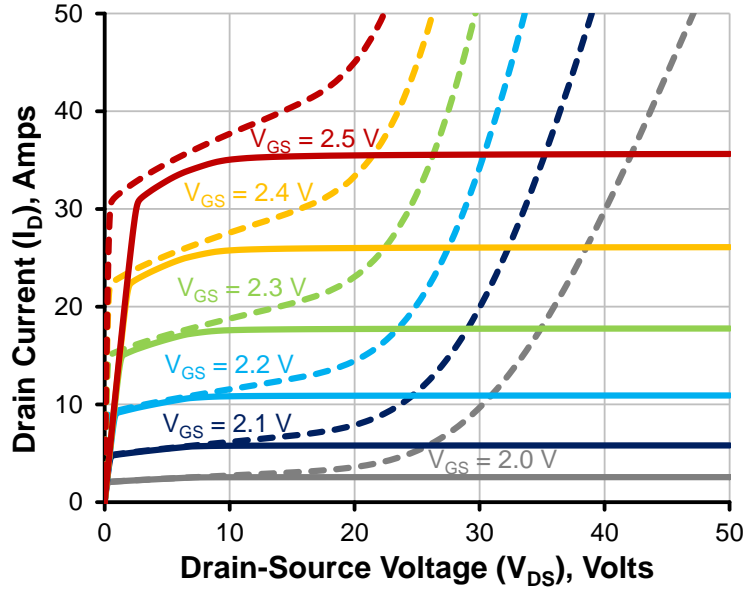
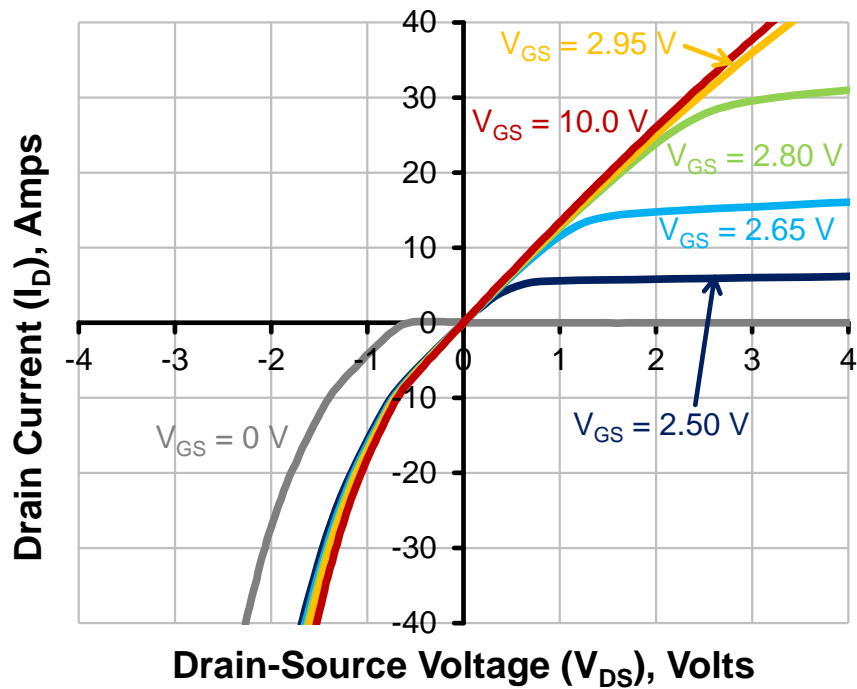


Figure 5.2: Simulated divergence between SJDP120R085/FDMS5352 cascode (solid lines) and FDMS5352 I-V curves (dashed lines). The cascode curves do not curve upward at higher V_{DS} .

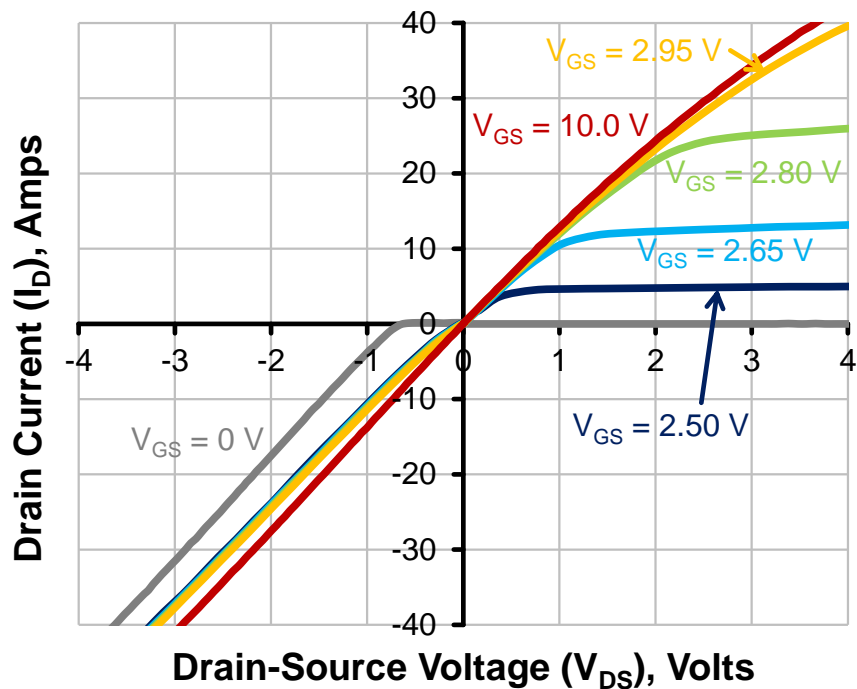
starts blocking voltage. For higher $V_{DS(casc)}$, the I-V curve is completely flat, since the HV device prevents any further rise of $V_{DS(LV)}$ and no breakdown behaviour of the LV switch is observed.

Simulation example It is difficult to measure the point at which the cascode saturation characteristics level off as they are clamped by the HV transistor. This is due to the unavoidable self-heating effects of making measurements at high V_{DS} . However, this behaviour is easy to model in SPICE.

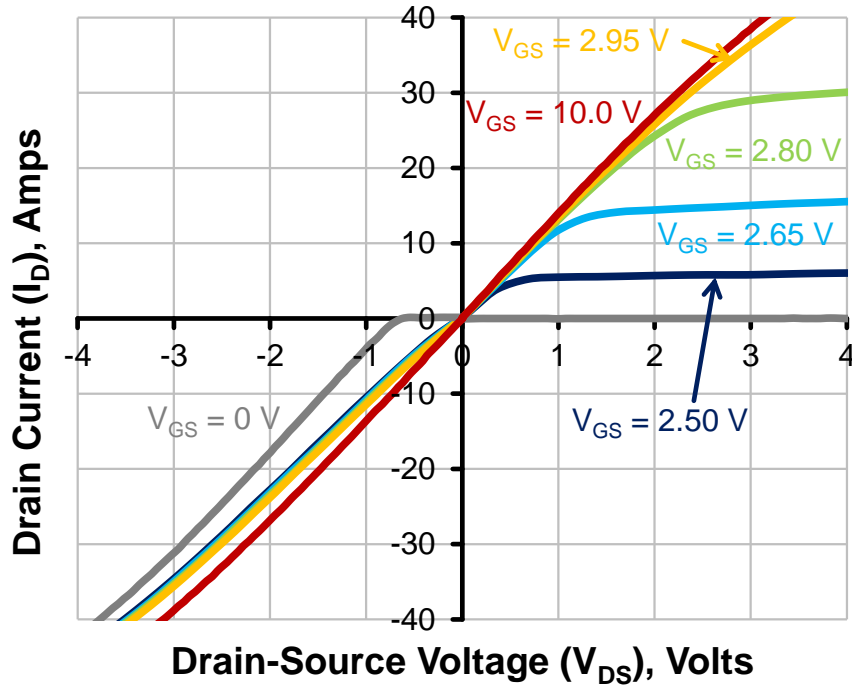
Figure 5.2 shows the simulated forward I-V characteristic of the SiC JFET/Si MOSFET cascode of chapter 4, compared to the I-V characteristics of the LV MOSFET alone. The point at which the JFET starts to block $V_{DS(casc)}$ can be seen, where the two sets of traces begin to diverge at around $V_{DS} = 10$ V. Note also that the slope of the linear region in the cascode simulation is clearly limited by the JFET $R_{DS(ON)}$.



(a) Si SJ MOSFET



(b) SiC MOSFET



(c) SiC JFET

Figure 5.3: I-V curves for cascode devices in forward and reverse conduction

The independent nature of the linear and saturation regions of the cascode circuit allows arbitrary combinations of devices to be combined to achieve a desirable combination of on-state characteristics and threshold voltage.

5.3.2.2 Reverse conduction (third quadrant of I-V curve)

Reverse conduction mechanism Cascode reverse conduction is a very different process to reverse conduction in a conventional transistor. If the cascode switch is turned off, only a small negative $V_{DS(casc)}$ is required to forward bias the LV MOSFET body diode, since the HV transistor channel becomes fully-enhanced under these conditions. As soon as this happens, the drain of the LV MOSFET and the source of the HV device are clamped to the cascode source. Since the gate bias for the HV device must ensure that the HV transistor becomes fully enhanced when $V_{DS(LV)} \approx 0$, as soon as the LV MOSFET body diode is forward biased, current is able to flow through it and continue through the now fully-enhanced HV device.

Implications of reverse conduction behaviour The reverse conduction behaviour of the cascode switch therefore has approximately the reverse conduction I-V characteristic of the fully-enhanced HV device, shifted by the LV MOSFET body diode forward voltage, provided

the LV MOSFET channel is not conducting. Due to the low V_f of the LV MOSFET body diode, reverse conduction through the HV transistor takes place in a manner similar to synchronous switching. Although the LV MOSFET body diode is a P-N junction diode and will therefore experience reverse recovery, it is a LV device and its contribution to switching losses will be small. Furthermore, it may be feasible to bypass the LV MOSFET body diode with a parallel LV Schottky diode and reduce or eliminate these undesirable effects completely. Synchronously switching the LV MOSFET gate to coincide with reverse conduction could also avoid this problem.

One possibly undesirable characteristic of cascode circuits is that reverse conduction is unavoidable when $V_{DS(casc)}$ becomes negative. A HV SiC Schottky diode does not have sufficiently low forward voltage drop to completely avoid reverse conduction through the cascode circuit at any significant current. For both the Si SJ MOSFET and SiC MOSFET, this means that their own body diodes would also become forward biased.

Although the body diode may not carry the majority of the current, this could still lead to reverse recovery losses. In contrast, a benefit of the JFET cascode is the guarantee that all reverse conduction current is carried in the JFET channel itself.

The use of cascode reverse conduction as a free-wheel mechanism is discussed further in section 5.4

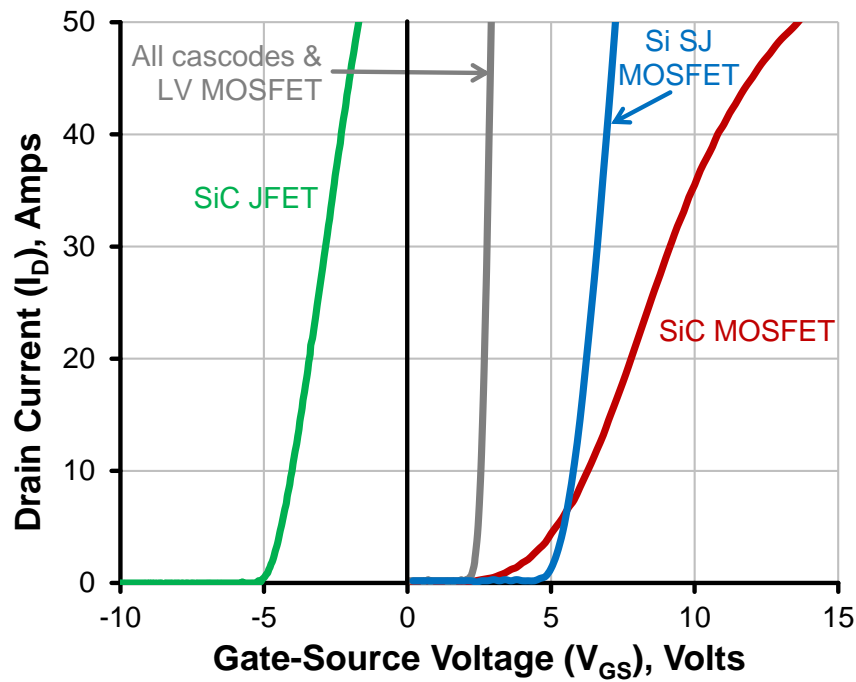
5.3.3 Transfer characteristics

The transfer characteristics (I_D vs V_{GS}) for each device combination are shown in figure 5.4a. From these data, the maximum slope of each line was calculated to determine the peak g_m of each device. This is summarised in figure 5.4b.

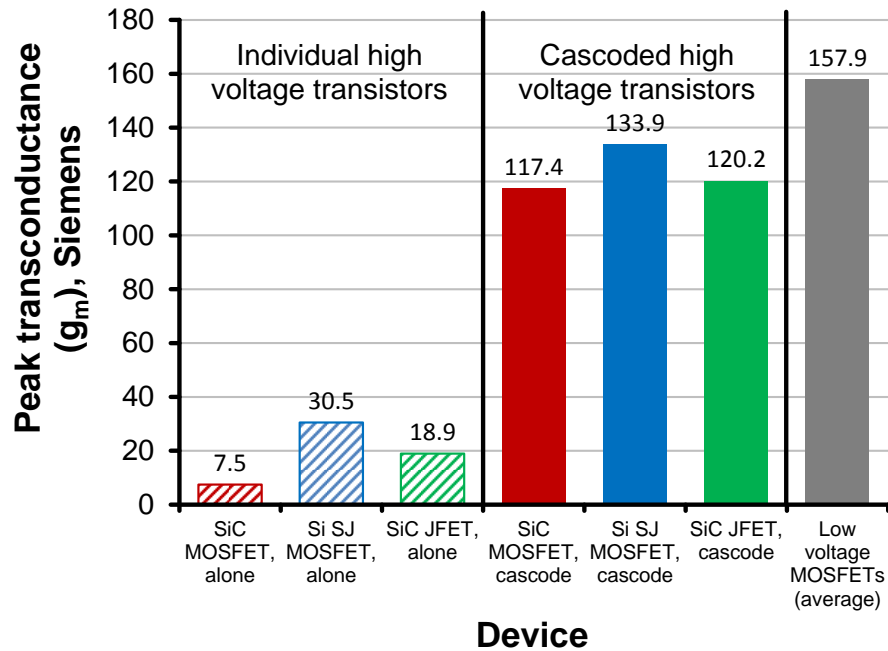
The wide variations between the properties of the different HV FETs is obvious in both figures. The depletion mode transfer characteristic of the SiC JFET is apparent by its location in the left-half plane of figure 5.4a, whilst the low V_T of the SiC MOSFET is also noticeable, with a value around half that of the Si SJ MOSFET. The different gradients of the HV FET transfer characteristics indicate a wide variation in g_m . This becomes particularly clear in figure 5.4b, which shows that the Si SJ MOSFET has a g_m four times greater than that of the SiC MOSFET, whilst the SiC JFET g_m is about half way between the other two HV devices. The variation in carrier mobility that causes this effect was explained in section 5.3.1.1.

In the cascode configuration, the transfer characteristics of the three HV devices are indistinguishable from that of the LV Si MOSFET. In figure 5.4a, it is necessary to represent them all with a single line.

A small amount of variation in g_m between the cascode devices is visible in figure 5.4a, since these data were extracted mathematically from the peak $\frac{dI_D}{dV_{GS}}$ for each individual curve.



(a) Transfer characteristics



(b) Peak transconductance

Figure 5.4: Gate control characteristics at $V_{DS} = 10$ V for all devices combinations

The transconductance of the cascode devices is much greater than for the individual FETs and approaches that of the LV Si MOSFET.

These transfer characteristics illustrate an interesting property of cascode circuits: that their transfer characteristic is determined almost entirely by the LV device. This means that no matter what HV transistor is used in a cascode circuit, the threshold voltage and transconductance may be set arbitrarily, simply by careful selection of the LV device.

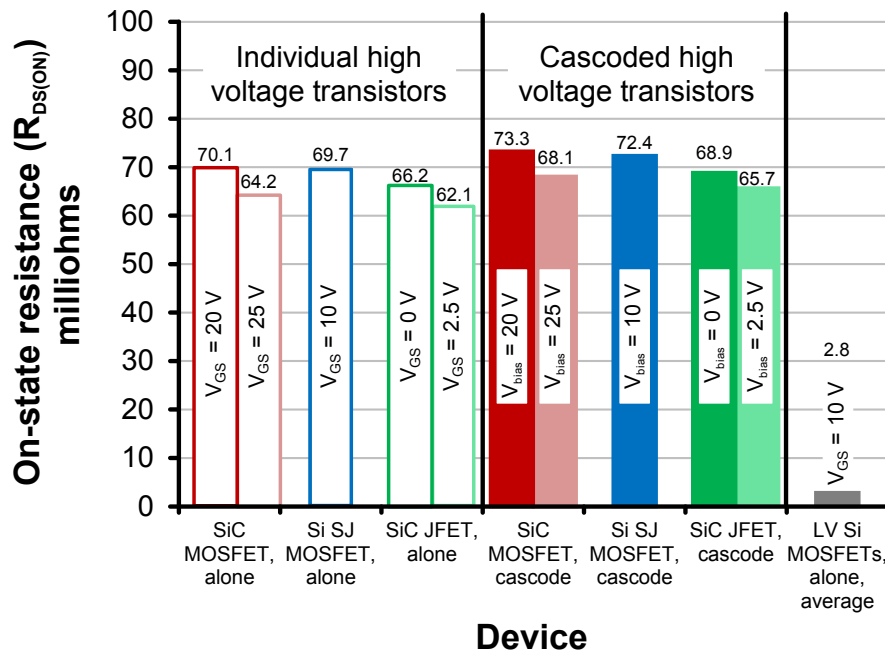


Figure 5.5: $R_{DS(ON)}$ for all device combinations at $V_{DS} = 0\text{ V}$. All cascode measurements were taken with $V_{GS(LV)} = 10\text{ V}$

5.3.4 On-state resistance

The on-state resistance of each individual and cascode device was measured using a precision multimeter at $V_{DS} = 0$ V and averaged over 10 readings. Kelvin connections were used due to the very low DC resistance of the devices.

Due to the low g_m of the SiC MOSFET, measurements were taken with its gate biased at both the manufacturer's recommended value of 20 V and at its gate-source rating of 25 V. Measurements of the SiC JFET $R_{DS(ON)}$ were taken at a gate bias of 0 V, often used for its ease of implementation and at 2.5 V, close to the onset of gate diode conduction. The Si SJ MOSFET was measured only at the recommended value of $V_{GS} = 10$ V, since further increases in gate voltage can do little to further enhance the channel. These measurements are summarised in figure 5.5.

As would be expected, using a HV transistor in a cascode configuration simply increases the overall $R_{DS(ON)}$ by that of the LV device: in this case around 3 m Ω . Using the HV devices investigated here in a cascode configuration therefore increases on-state losses by between 4 and 6%.

The effect of V_{GS} on $R_{DS(ON)}$ is also interesting. Operating the SiC MOSFET at $V_{GS} = 25$ V reduces on-state losses by around 8% compared to operation at $V_{GS} = 20$ V. Although this is a useful improvement, it is impractical, since it is the rated voltage of the gate.

Operating the SiC JFET at $V_{GS} = 2.5$ V reduces on-state losses by around 5% compared to operation at $V_{GS} = 0$ V. Although the reduction in $R_{DS(ON)}$ is not large, operation at $V_{GS} = 2.5$ V is practical and easy to implement, particularly in the cascode configuration. Operating the JFET cascode with a gate bias of 2.5 V entirely compensates for the increased $R_{DS(ON)}$ of the cascode arrangement, compared to an individual JFET operated at $V_{GS} = 0$ V. The benefits of higher gate voltage are reduced slightly when operating in the cascode configuration.

$R_{DS(ON)}$ is an important consideration for on-state losses, but these results show that any increased losses due to the use of cascoded transistors are small, provided devices are chosen appropriately. The magnitude of $R_{DS(ON)}$ can be altered slightly depending on the choice of HV gate voltages. However, both of these effects are marginal compared to the influence of temperature and current on $R_{DS(ON)}$, which is discussed in section 5.5.

5.4 Cascode reverse conduction as a free-wheel path

Many switch-mode converter topologies require a suitable 'free-wheel' path for inductor current as the power transistors switch from conducting current to blocking it. The free-wheel path is ideally lossless and capable of switching instantly. In some topologies, particularly bridge converters, the free-wheel path is in inverse-parallel with the power transistors and their

channel or body diode can be used in place of an external diode. This reduces the component count and may reduce losses.

Whilst reverse conduction through power transistors is an established technique for silicon MOSFETs, it has only been described briefly for cascode devices [73, 135]. In this section, the properties of different conventional free-wheel mechanisms are discussed and compared with the properties of cascode reverse conduction.

5.4.1 Existing reverse conduction techniques

5.4.1.1 High voltage diodes

HV silicon diodes suffer from significant series resistance and poor reverse recovery performance due to the large number of carriers stored in the intrinsic region. They therefore experience a forward voltage drop of several volts at high current, which reduces their efficiency [186].

Schottky diodes have lower forward voltage drop than P-N junction diodes and a near-zero reverse recovery time¹. However, silicon Schottky diodes are unable to block more than around 200 V, so it is necessary to use SiC Schottky diodes at higher voltages which have higher forward voltages than their silicon counterparts.

5.4.1.2 Body diodes

Power MOSFETs and some other devices have an intrinsic inverse parallel body diode as a result of the structure of the semiconductor. The body diode may be used in place of an external diode and is usually capable of handling very high currents. However, it can often exhibit poor reverse recovery performance. Nevertheless, it is a cheap and convenient solution: commutation through a body diode is automatic and does not complicate gate drive control schemes.

5.4.1.3 Synchronous switching

Synchronous switching can improve reverse conduction performance compared to the use of external or body diodes by allowing current to flow through the device channel when V_{DS} is negative. For high current devices with low channel resistance, this can be substantially more efficient than using discrete free-wheel diodes due to lower reverse recovery losses, but care must be taken that V_{DS} is insufficient to forward bias the body diode. Synchronous switching

¹Reverse recovery current exists solely due to the capacitive nature of the diode junction, rather than the presence of carriers in the depletion region

complicates gate drive control schemes by requiring more switching events and careful control of dead-time.

5.4.2 Reverse conduction characteristics

The passive reverse conduction characteristics of the three HV transistors were measured for the devices operating individually and in the cascode configuration. Additionally, the synchronous reverse conduction behaviour for the same devices in cascode configuration was also investigated. In each case, the conduction characteristic of a Cree C4D20120D 34 A, 1200 V SiC Schottky diode is included for comparison. This device has similar current ratings to the transistors being investigated and is representative of a discrete SiC Schottky diode that might be used in conjunction with any of these devices.

5.4.2.1 Individual devices: passive reverse conduction

Figure 5.6a compares the body diode characteristics of the individual HV devices measured for $V_{GS} = 0$ V. The body diode characteristic of the LV Si MOSFET is also shown. Since the SiC JFET has no body diode mechanism, its reverse conduction characteristic at $V_{GS} = -5$ V is instead plotted for comparison. This is an unlikely operating point as it provides no noise immunity. However, it is included as a ‘best case’ because it represents the lowest loss passive reverse conduction mechanism that still enables the JFET to be turned off fully.

Si SJ MOSFET None of the individual HV devices have reverse conduction characteristics that are attractive as a current free-wheel path. The Si SJ MOSFET body diode has by far the lowest static losses, with a forward voltage drop of only around 1 V at rated current. However, SJ body diodes are well-known for their problematic reverse recovery behaviour, so the low static loss in this case must be considered in the context of significant expected switching losses.

SiC Schottky diode The discrete SiC Schottky diode has a slightly higher V_f than the Si SJ MOSFET body diode and exhibits a modest slope, indicating comparatively high series resistance. Despite this rather lacklustre on-state performance, the negligible reverse recovery of the SiC Schottky diode is likely to have distinctly better HV switching performance compared to the Si SJ MOSFET body diode. However, it is unable to act as a substitute reverse conduction path for the Si SJ MOSFET, since the lower V_f of the SJ MOSFET body diode ensures it carries the majority of the current regardless.

SiC MOSFET The body diode characteristic of the SiC MOSFET is an extremely lossy reverse conduction path due to its high V_f and slow initial rate of rise of I_S with V_{SD} . In addition, the body diode is a P-N device and is therefore likely to show reverse recovery behaviour [67], although these are not as severe as in Si SJ devices. For an individual SiC MOSFET, it is therefore preferable to use a SiC Schottky diode in inverse parallel as a free-wheel path, although this will only reduce and not eliminate body diode reverse recovery effects.

SiC JFET It is not practical to ensure a passive reverse conduction path through the SiC JFET without serious compromises to either reverse conduction losses or noise immunity. Even at the threshold shown in figure 5.6a, the reverse conduction characteristic is poor and very lossy. However, this does make it practical to use an inverse parallel SiC Schottky diode for reverse conduction. This is a much more attractive option for the JFET than the SiC MOSFET, since the absence of any body diode ensures negligible reverse recovery [75].

5.4.2.2 Cascode: passive reverse conduction

Figure 5.6b compares the reverse conduction characteristics for the cascoded devices measured for $V_{GS(LV)} = 0$ V. V_{bias} on the HV transistor gates was 20 V, 2.5 V and 10 V for the SiC MOSFET, SiC JFET and Si SJ MOSFET respectively. This ensured that all devices were fully-enhanced in the on-state.

The reverse conduction characteristics of all three HV cascodes share many similarities, particularly when conducting less than 10 A, due to their closely-matched HV channel resistances.

Si SJ MOSFET The reverse conduction behaviour of the Si SJ MOSFET cascode is poor compared to that of the standalone device. At rated current, V_{SD} is more than doubled compared to operating the same Si SJ MOSFET alone. In addition, the HV SJ body diode is unavoidably forward biased, so there is no reduction in reverse recovery losses.

Although the cascode configuration may have benefits for switching HV Si SJ devices, its reverse conduction characteristics are very poor. The use of an anti-parallel SiC Schottky diode could partially reduce both static and reverse recovery losses. However static losses would still be higher than for an individual Si SJ MOSFET and reverse recovery losses would still be substantial.

SiC devices Both HV SiC cascodes have very similar passive reverse conduction characteristics, both of which are significantly better than those of either of the individual SiC tran-

sistors: at 25 A, the static losses in both cases are reduced by around 25 %. This is because conduction through the channel dominates in these cascode devices.

For the SiC MOSFET cascode the additional voltage drop across the LV body diode ensures that the SiC MOSFET body diode conducts only a small proportion of the total current, around 10 % at 25 A. This minimises reverse recovery losses in the SiC MOSFET. The lack of an intrinsic reverse conduction path ensures that the JFET experiences negligible reverse recovery losses. Some reverse recovery losses will occur due to conduction through the LV MOSFET body diode in both cascodes, but this should be small, due to the low voltage rating of this transistor.

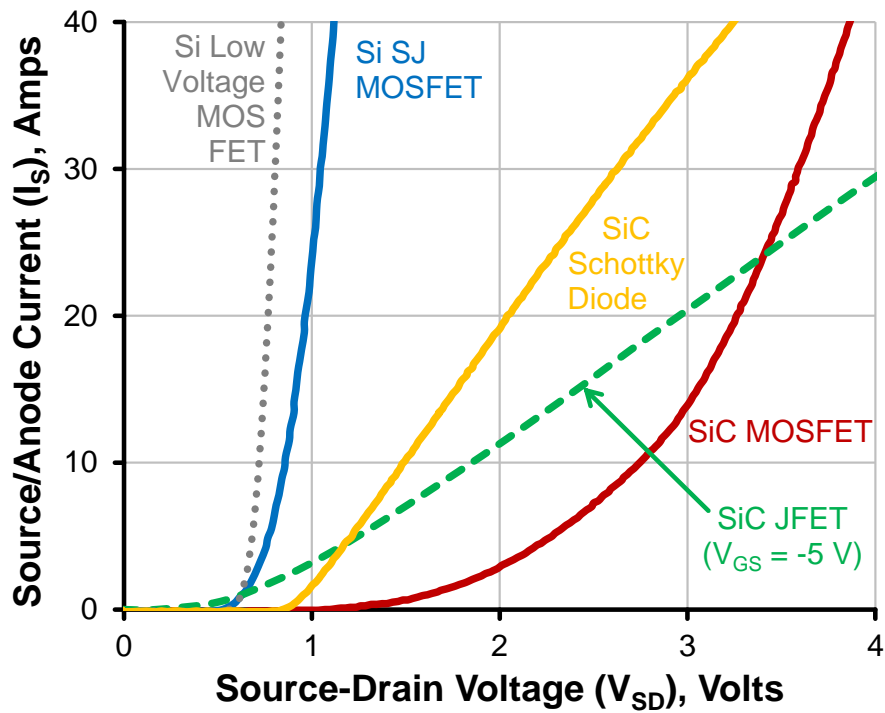
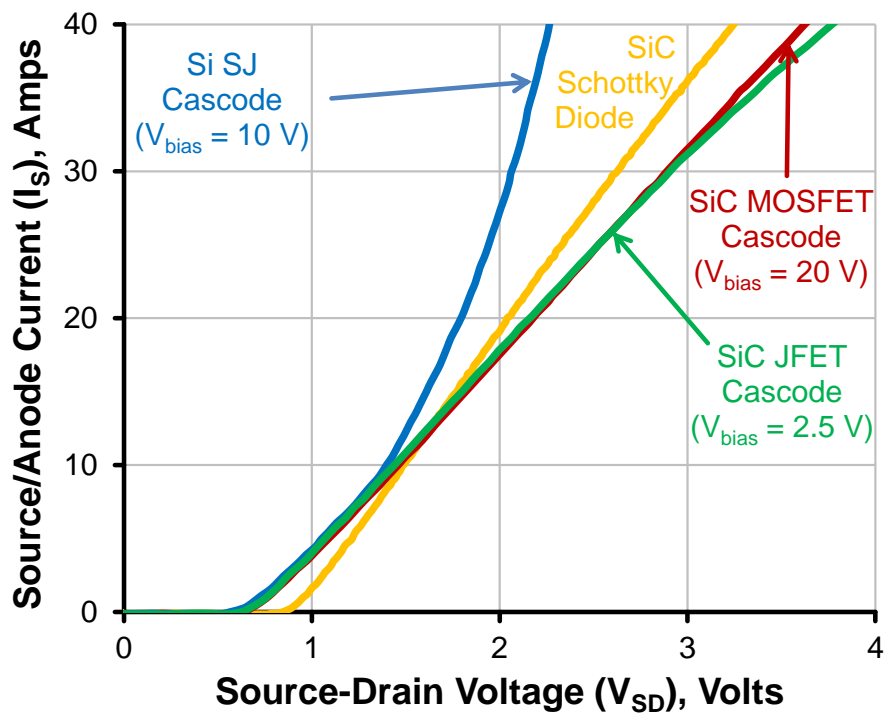
It is important to note the similarity between the passive reverse conduction characteristics for the SiC cascodes compared to that of the SiC Schottky diode. Static losses are similar over most of the current range, with cascode losses being lower below 10 A, but overtaking the Schottky diode losses as current increases. At 25 A, cascode static losses are around 10 % higher for the cascodes than for the Schottky diode. However, natural commutation through a SiC cascode switch is largely competitive with the performance of a SiC Schottky free-wheel diode.

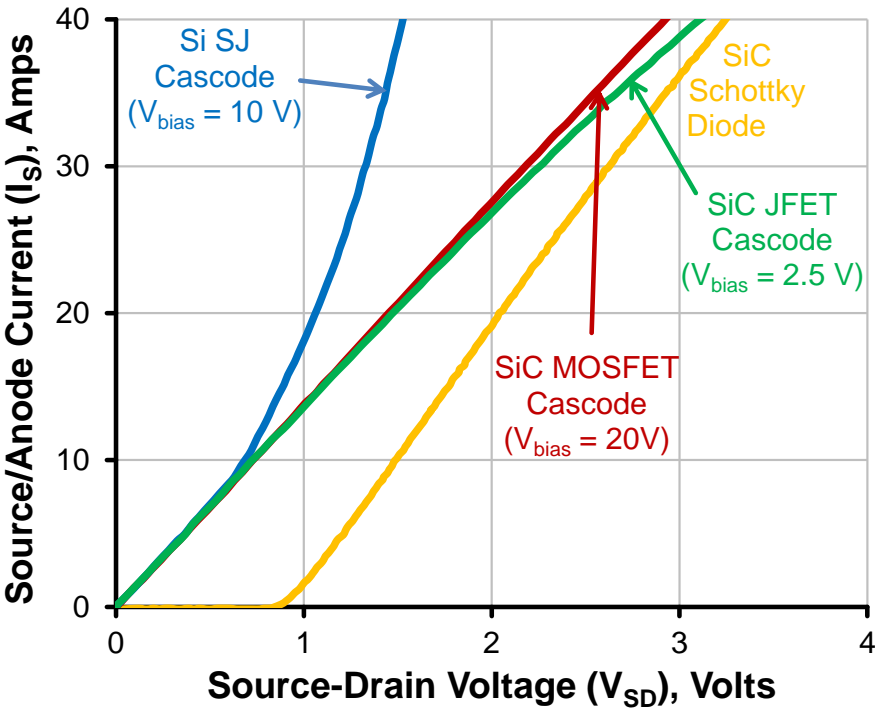
Advantages Passive reverse conduction through a WBG cascode has several advantages. It eliminates an additional, expensive component, which reduces the required board area and simplifies heatsinking; indeed the cost saving from eliminating a SiC Schottky diode could easily be invested in a lower $R_{DS(ON)}$ HV transistor, resulting in both lower forward and reverse conduction losses. The absence of a SiC Schottky diode can also slightly reduce switching losses, since it reduces the effective transistor C_{oss} , which is discharged lossily once per switching cycle. Both switching and static losses in reverse conduction could feasibly be reduced still further by the addition of a low cost LV Si Schottky Diode in inverse parallel with the LV MOSFET. This could slightly reduce static losses and potentially eliminate reverse recovery losses in the LV MOSFET body diode.

5.4.2.3 Cascode: synchronous reverse conduction

Synchronous reverse conduction, in which the device is turned on to coincide with the period of reverse current is also possible in cascode devices. Figure 5.6c shows the active reverse conduction characteristics of the same three cascode devices described previously for $V_{GS(LV)} = 10$ V.

Thanks to the very small $R_{DS(ON)}$ of the LV MOSFET, the active reverse conduction characteristics of the cascodes are similar to those of the passive ones, less the forward voltage drop of the Si MOSFET body diode. They are also almost indistinguishable from the active

(a) Individual HV devices and LV Si MOSFET, $V_{GS} = 0$ V (Except JFET)(b) Cascoded HV devices, $V_{GS(LV)} = 0$ V



(c) Cascoded HV devices, $V_{GS(LV)} = 10\text{ V}$

Figure 5.6: Reverse conduction characteristics for individual and cascoded high voltage devices

reverse conduction characteristics of the individual devices. The lower forward voltage drop corresponds to a reduction in static losses of around 30% at 25 A and leads to lower losses compared to the use of the SiC Schottky diode across the entire current range.

Lower on-state losses are an obvious benefit of synchronously switching a cascode, although a slightly more complex switching scheme is required. However, for SiC cascades the passive reverse conduction mechanism is not unattractive and the transition from passive to active reverse conduction also is straightforward: the LV MOSFET only has to switch the forward voltage of its body diode.

A conservative approach could therefore be taken in which the cascode is allowed to commute passively before being switched actively. This would allow some of the benefits of synchronous rectification to be exploited without the need to measure current or voltage waveforms very precisely.

5.4.3 Problems with cascode reverse conduction

Some care must be taken with device ratings during cascode reverse conduction. Under these conditions, the gate-drain voltage V_{GD} is described by: $V_{GD(HV)} = V_{bias} + V_{f(LV)} + V_{SD(HV)}$. Hence increasing reverse conduction current leads to increasing V_{GD} . Maximum ratings for V_{GD} are rarely provided by manufacturers, but due to the approximately symmetrical nature of FET channels, it is reasonable to suggest that $V_{GD(max)}$ will be similar to $V_{GS(max)}$.

Both SiC devices require a gate bias close to rated limits for optimum on-state performance; the SiC MOSFET gate must operate close its breakdown voltage and the SiC JFET gate diodes at the point of forward conduction to minimise channel resistance. This provides limited margin for reverse conduction. Hence, utilising cascoded devices in reverse conduction mode requires a trade-off with on-state performance, although the benefits of cascode reverse conduction may make this worthwhile.

5.5 High temperature operation

Interest in the very high temperature capabilities of WBG power devices has waned in the last few years due to efficiency and reliability concerns, as described in section 2.3.3. Nevertheless, it is helpful to examine the behaviour of SiC devices over an extended temperature range, since variations in high temperature performance between devices can affect their suitability for different applications.

In this section, the dependence of $R_{DS(ON)}$ and V_T on temperature for the SiC MOSFET and JFET studied previously, as well as the JFET gate diode forward voltage, are investig-

ated over a temperature range of 25 to 200 °C. This temperature range exceeds the 150 °C rated operating range of both devices. However, temperature ratings are often determined by device packaging, rather than the semiconductor itself and these measurements provide a useful comparison of the high temperature behaviour of the SiC JFET and MOSFET.

5.5.1 Experimental set-up

To test each device at high temperature, its TO-247 package was bolted to a large heatsink, with a 100 W power resistor mounted on the opposite side to heat the assembly. The assembly could also be cooled by forced convection from a fan mounted on top of the heat sink fins. Device temperature was measured using a K-type thermocouple thermally bonded to the transistor's thermal tab. Heat transfer compound was used to ensure good thermal conductivity throughout. The heatsink temperature set by a commercial temperature controller which adjusted the power supplied to the power resistor and fan to achieve and maintain the required temperature.

The SiC transistor characteristics were measured using a Tektronix 371A curve tracer at intervals of 25°C between 25 and 200 °C, after the temperature had stabilised to within ± 1 °C of the set point. Since self-heating of the transistor was minimised due to the pulsed nature of the measurements, the transistor die temperature can be assumed to have remained very close to the heatsink temperature throughout.

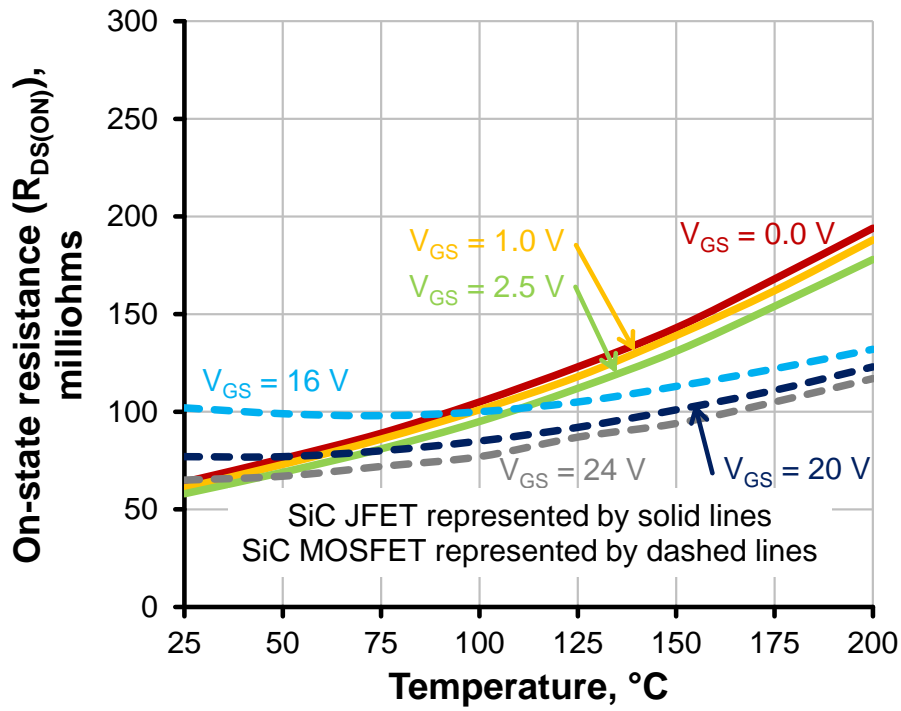
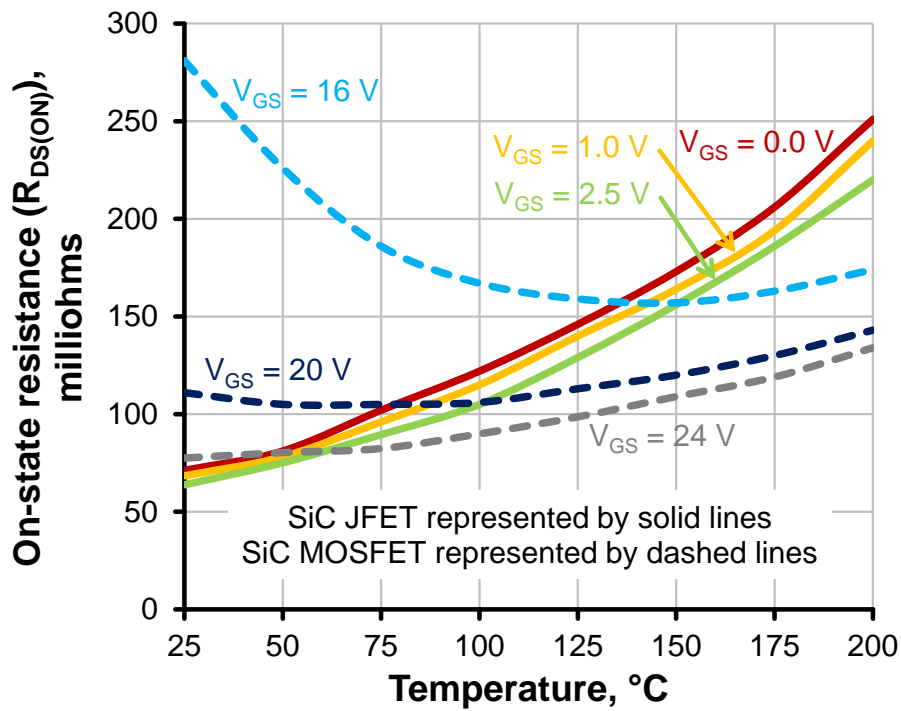
5.5.2 Experimental results

5.5.2.1 On-state resistance

Figure 5.7 shows how $R_{DS(ON)}$ changes with temperature for the SiC MOSFET and JFET. Measurements were taken at both $I_D = 1$ A and 20 A, as there can be a strong dependence of $R_{DS(ON)}$ on I_D [191]. $R_{DS(ON)}$ for each device is plotted for three values of V_{GS} which are large enough to ensure a well-enhanced channel.

At 1 A the JFET $R_{DS(ON)}$ increases approximately exponentially with temperature; over the full temperature range, $R_{DS(ON)}$ triples. In contrast, the SiC MOSFET appears to have a more stable $R_{DS(ON)}$ with temperature, which does not increase exponentially and is approximately constant at lower temperatures. However, the effect of V_{GS} on $R_{DS(ON)}$ is not consistent and reduces with increasing temperature.

The variation in the relationship between $R_{DS(ON)}$ and V_{GS} for the SiC MOSFET might be assumed to be due to g_m varying with temperature. However, figure 5.8, which plots the change in the transfer characteristic of the SiC MOSFET with temperature over the same

(a) $I_D = 1\text{ A}$ (b) $I_D = 20\text{ A}$ Figure 5.7: $R_{DS(ON)}$ for SiC MOSFET and SiC JFET from 25 - 200 $^{\circ}\text{C}$

temperature range, shows that each curve has a similar gradient, implying that g_m changes only slightly. Increasing temperature does, however cause the curves to be shifted along the x-axis, indicating that this variation is due to V_{th} falling with increasing temperature.

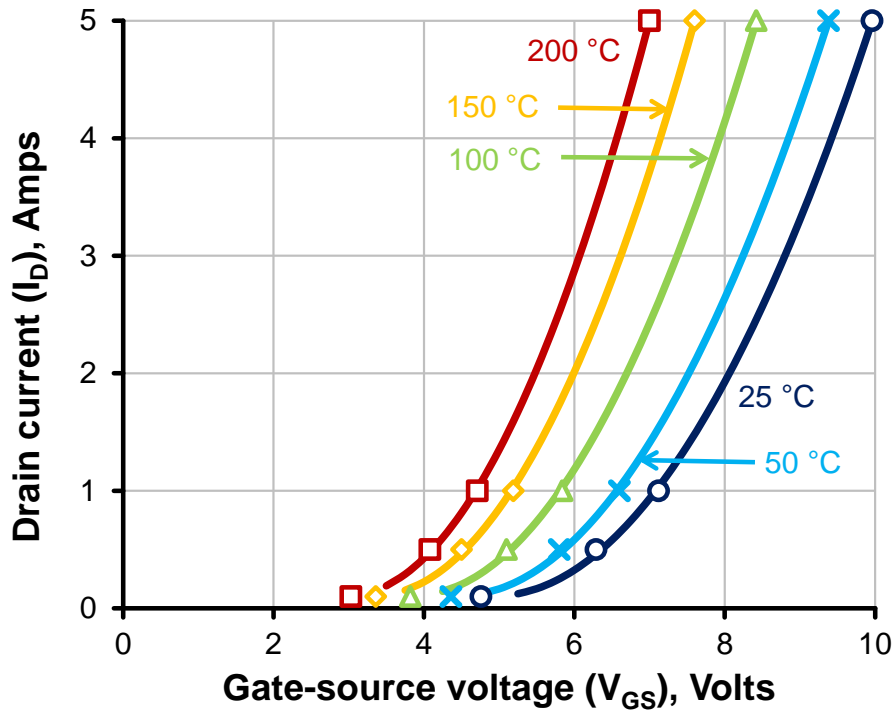


Figure 5.8: Change in SiC MOSFET transfer characteristic from 25 to 200 °C for $V_{DS} = 10$ V. Solid lines are quadratic lines of best fit for the data points.

5.5.2.2 Threshold voltage

The effect of temperature on V_T for both devices is shown in figure 5.9. Both devices experience substantial falls in V_T as temperature increases, although the SiC MOSFET fares worse, with a fall in V_T of more than twice that of the JFET over its rated operating temperature range.

This can be particularly problematic for the SiC MOSFET, since it significantly reduces its noise immunity at turn-off. For this reason, Cree recommend a negative gate bias at turn-off [67], which can complicate the gate drive circuit. Although V_T for the JFET also falls with increasing temperature, little effect can be seen in figure 5.7. Thanks to its larger g_m , all the values of V_{GS} plotted are sufficient to almost fully enhance the channel and the fall in V_T does not change this.

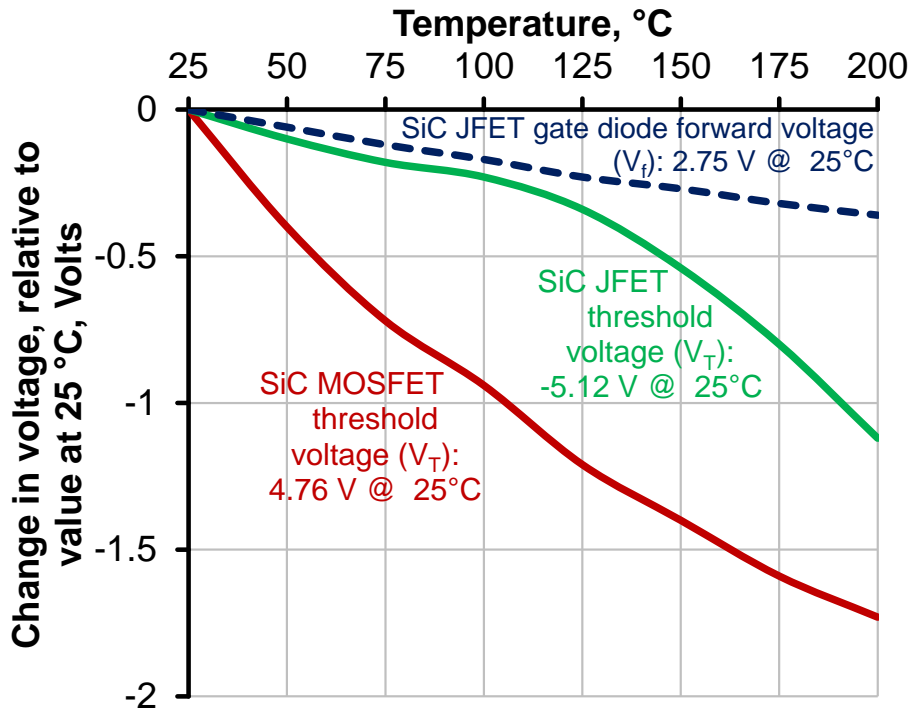


Figure 5.9: Change in V_T at $I_D = 100$ mA for SiC MOSFET and SiC JFET and change in JFET gate-source diode V_f at $I_G = 100$ mA from 25 to 200 °C.

5.5.2.3 JFET gate-source diode

Figure 5.9 also shows that the forward voltage of the JFET gate-source diode falls as temperature rises. This is significant because it limits the effectiveness of increasing V_{GS} to reduce

$R_{DS(ON)}$ at higher temperatures. Whilst operating the JFET on the cusp of gate-source diode conduction will provide a slightly lower $R_{DS(ON)}$ at 25 °C, this advantage is quickly reduced as temperature increases, unless significant gate current is supplied by the gate driver. A high gate current increases on-state and gate driver losses and is likely to counteract any advantage from reduced $R_{DS(ON)}$.

5.5.2.4 Drain current

The effect of I_D on $R_{DS(ON)}$ is also significant, as can be seen by comparing figures 5.7a and 5.7b. In all cases, operation at higher currents increases $R_{DS(ON)}$, particularly at elevated temperatures. This is especially true of the SiC MOSFET, for which the curves are drastically altered.

A comparatively large change in V_{GS} is required to saturate the channel of both SiC transistors. Since the SiC MOSFET is only just fully-enhanced at $V_{GS}=20$ V, different values of I_D can lead to large changes in $R_{DS(ON)}$ because of the soft transition between the linear and saturation regions for this device. This can be seen in figure 5.1. In a practical application, this means that the SiC JFET is likely to be more competitive with the SiC MOSFET in terms of $R_{DS(ON)}$ than measurements taken at low current, such as figure 5.7a would suggest, due to its superior g_m .

5.5.2.5 Specific on-state resistance

It could be argued that these devices may constitute an unreasonable comparison. The relatively small variation of $R_{DS(ON)}$ with temperature for the SiC MOSFET is due to its poor channel mobility. Consequently, the specific on-state resistance of the SiC MOSFET die is far greater than that of the SiC JFET, hence the die area is proportionally larger as well.

Based on the $R_{DS(ON)}$ obtained in figure 5.5 and the die dimensions from the manufacturer's datasheets [192, 193], the SiC JFET has a specific $R_{DS(ON)}$ of $3.35 \text{ m}\Omega\text{cm}^{-2}$ at $V_{GS} = 2.5$ V compared to $6.68 \text{ m}\Omega\text{cm}^{-2}$ at $V_{GS} = 25$ V for the SiC MOSFET. For a given die size therefore, a similar SiC JFET could be expected to have an $R_{DS(ON)}$ half that of a similar SiC MOSFET. This may be seen very clearly in figure 5.10, in which the data from figure 5.7a are redrawn in terms of specific $R_{DS(ON)}$.

These are important considerations in high power density applications, for which bare dies are used. However, since this comparison is concerned with devices of similar ratings in the same package, specific $R_{DS(ON)}$ is not relevant, except to explain device behaviour.

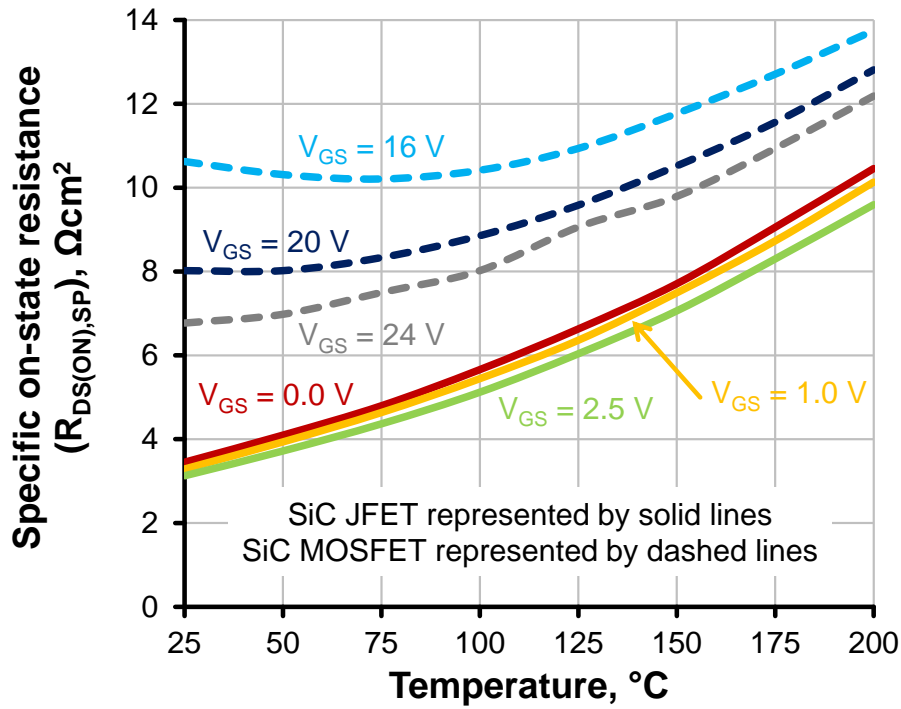


Figure 5.10: Temperature dependence of specific $R_{DS(ON)}$ for SiC devices at 1A from 25 to 200 °C

5.5.3 Implications of temperature for SiC device operation

The significant increase in JFET $R_{DS(ON)}$ clearly limits its suitability for high temperature operation without substantial de-rating. In contrast, the MOSFET sees a much smaller rise in $R_{DS(ON)}$ over the temperature range, making it appear to behave more consistently and have noticeably lower $R_{DS(ON)}$ from temperatures as low as 50 °C.

Some caution must be applied to such a simple comparison. Under more realistic operating conditions of perhaps $I_D = 20$ A and $V_{GS} = 2.5$ V for the JFET and $V_{GS} = 20$ V for the MOSFET, $R_{DS(ON)}$ for the JFET is competitive with that of the MOSFET to at least 100 °C. This is due to the need to avoid operation close to the MOSFET gate-source breakdown voltage and the dependence of its $R_{DS(ON)}$ on I_D .

The sometimes negative temperature coefficient of the MOSFET $R_{DS(ON)}$ visible in figure 5.7 is a concern in high current applications where current sharing between several devices is necessary. Without a consistently positive temperature coefficient, current sharing between SiC MOSFETs is likely to be unstable and this is exacerbated by the dependence of the temperature coefficient on I_D .

In high power density applications where current sharing is required, the JFET is a much better choice, as a result of the positive temperature coefficient of its very low specific $R_{DS(ON)}$.

5.6 Static characteristics: conclusions

The experimental work in this chapter has highlighted the unique static characteristics of the power cascode. Although the cascode configuration necessarily increases overall $R_{DS(ON)}$, this effect is small compared to changes in $R_{DS(ON)}$ due to variations in temperature or $V_{GS(ON)}$. It can also be mitigated in some cases by careful choice of HV bias voltage.

Using a cascode circuit, it becomes possible to arbitrarily alter g_m and V_T based on the selection of LV device, whilst independently adjusting $R_{DS(ON)}$ based on the selection of the HV device. The saturation region characteristics of the cascode circuit are also extremely consistent, from the V_{DS} at which the HV transistor begins to switch, to the point at which it breaks down.

SiC JFETs and MOSFETs can particularly benefit in a cascode circuit, as it compensates for their otherwise undesirable V_T and g_m characteristics, whilst offering an attractive passive commutation mechanism with comparable performance to a SiC Schottky diode. The Si SJ MOSFET does not benefit from being used in a cascode circuit and doing so is likely to increase overall losses.

Investigation of the high temperature performance of the SiC devices supports the suggestion that such operating points are for reasons of efficiency. Although the SiC MOSFET will experience lower on-state losses than the JFET at higher temperatures, its performance is hampered by the dependence of its $R_{DS(ON)}$ on I_D and its negative V_T temperature coefficient.

In high current applications using parallel-connected devices, the JFET is preferred for its low specific $R_{DS(ON)}$ and its current sharing properties, even at high temperatures.

Chapter 6

Dynamic characteristics

6.1 Introduction

To have a complete picture of the operation of a cascode circuit, it is important to understand its switching performance, as well as its static characteristics. This then makes it possible to accurately estimate switching as well as on-state losses.

In this chapter, the dynamic characteristics of the cascode circuit are considered. The switching characteristics of the same three devices discussed in the previous chapter are compared when operated individually and in the cascode configuration. The benefits and drawbacks of cascode dynamic operation are then quantified.

The effects of gate resistances on the control of switching are examined and experimental measurements are combined with SPICE model predictions to explain the inherent trade-offs of gate resistor selection. A similar study is performed for stray inductance, in which the advantages and disadvantages of stray inductance and the significance of its location are considered.

The chapter concludes by investigating the practicalities of $\frac{dV}{dt}$ control in cascodes, their susceptibility to $\frac{dV}{dt}$ interference and their reverse recovery behaviour.

6.2 Cascode switching performance

To investigate the implications of the cascode configuration on HV transistor switching performance, the same three HV devices investigated in the previous chapter were compared. Using a clamped-inductive switching circuit, the switching behaviour for each device was measured both individually and in a cascode configuration with a LV Si MOSFET.

6.2.1 Experimental set-up

6.2.1.1 Circuit set-up

To ensure similar operating conditions, the three HV devices used had identical TO-247 packages. Each circuit was constructed on an identical PCB with similar auxiliary components in the same physical arrangement.

This approach ensured that any significant variations between measurements could be directly attributed to the transistors used or the cascode arrangement, rather than to circuit parasitics or variations in measurement methods.

6.2.1.2 Gate drive

For each test, an optically-isolated double-pulse drive input was provided from the PIC signal generator as described in 3.3.2. In general, the LM5114 IC was used as the gate driver, mounted directly to the PCB as intended. The LM5114 has a pull-up resistance of $2\ \Omega$ and a pull-down resistance of $0.23\ \Omega$ [183]. For the silicon SJ MOSFET and for all the cascode switches, this was used to provide a gate drive voltage switching between 0 V and 10 V.

The same gate driver was used for the SiC JFET, but with its ground connection held at a -10 V relative to the JFET source, using an isolated power supply with common mode suppression. In this arrangement, the JFET gate signal could be switched between -10 V and +2.5 V.

The SiC MOSFET has higher voltage drive requirements than the other devices and it was not possible to drive its gate directly using the LM5114 without exceeding its voltage rating. Instead, a UCC27531 gate driver in a similar SOT23-6 package was used, supplied by a 20 V external isolated power supply and mounted immediately above the LM5114 IC to minimise any differences in parasitics between the ICs. The UCC27531 has a comparatively large pull-up resistance of $12\ \Omega$ and a pull-down resistance of $0.65\ \Omega$ [194]. In all cases, the gate drive voltages were those recommended by the device manufacturer.

6.2.1.3 Operating conditions

Each device combination was tested switching 25 A at 600 V. The 25 A switching current was chosen to ensure the transistors operated close to their current ratings, whilst the 600 V switching voltage permitted direct comparison between the 1200 V SiC devices and the 650 V silicon super-junction devices. Although the SiC devices are rated for considerably higher voltage operation, it is not necessary to operate near these voltage limits to benefit from their improved characteristics.

There was some variability in the peak turn-off current, depending on the delay between the control signal and start of the turn-off process: in some of the cascode switches, a large value of $R_{GL(LV)}$ is required to ensure stability and the inherently greater switching delay leads to slightly higher peak inductor currents. Fortunately, the inherently large time constant of the power inductor compared to the switching delay means that this error is limited to around 5% of rated current. The maximum error of V_{DC} was estimated to be approximately 2%.

6.2.1.4 Gate bias voltage

In the cascode configuration, each HV device requires a gate bias to ensure it is fully enhanced at turn-on. For the silicon SJ MOSFET, a gate bias of 10 V was used, to maximise channel enhancement, without being close to the gate voltage ratings. A 2.5 V gate bias was used for the SiC JFET to ensure maximum enhancement without the gate-source diode conducting.

The SiC MOSFET has a more problematic trade-off: the channel only becomes fully enhanced very close to the maximum rated gate voltage. Although using the highest possible gate voltage is desirable to minimise on-state losses, this is a hazardous operating point for the transistor. Therefore, for these measurements, a bias voltage of 20 V was used. This value is recommended by the manufacturer and ensures the transistor operates close to maximum enhancement, whilst providing a 5 V safety margin from the rated gate-source voltage of 25 V.

6.3 Comparative switching performance

6.3.1 Gate resistance

A different choice of gate resistors was required to control each device combination, due to their different characteristics. These were determined by experiment. The gate resistances chosen were those that minimised switching times whilst avoiding severe parasitic oscillations. Care was also taken to ensure V_{GS} and V_{DS} ratings of the devices were not violated.

Table 6.1 shows the gate resistances used for each arrangement. It should be noted that these gate resistances act in series with both the internal gate resistance of the device and any gate driver output resistance.

6.3.2 Switching behaviour

The switching characteristics of the three HV devices are shown for individual and cascode operation in figures 6.2 and 6.3 respectively. The time axes are arbitrary and $t = 0$ is defined

Device	R_{ON}	R_{OFF}	Device	$R_{GH(LV)}$	$R_{GL(LV)}$	$R_{G(HV)}$
Si SJ MOSFET	3.3 Ω	3.3 Ω	Si SJ MOSFET	4.7 Ω	300 Ω	1.5 Ω
SiC MOSFET	4.7 Ω	4.7 Ω	SiC MOSFET	1.5 Ω	10 Ω	4.7 Ω
SiC JFET	1.0 Ω	2.2 Ω	SiC JFET	0 Ω	4.7 Ω	4.7 Ω

(a) Individual power devices

(b) Cascode power devices

Table 6.1: Gate resistances used for control of standard and cascode switches

Device	C_{DG}	C_{iss}	C_{oss}	$R_{G(int)}$	V_{TH}	$V_{ON} - V_{TH}$	\hat{g}_m
Si SJ MOSFET	25 pF	5030 pF	70 pF	0.75 Ω	3.6 V	6.4 V	30.5
SiC MOSFET	7.6 pF	950 pF	82 pF	4.6 Ω	2.4 V	17.6 V	7.5
SiC JFET	35 pF	255 pF	0 pF	5.0 Ω	-4.8 V	7.3 V	18.9

Table 6.2: Device parameters relevant to switching. Capacitance is quoted for $V_{DS} = 600$ V [79, 145, 188]

at the point at which $V_{DS(casc)}$ begins to fall during turn-on and at which $V_{DS(casc)}$ reaches V_{DC} during turn-off. This allows direct comparisons to be drawn between the different traces.

All the traces show evidence of the stray capacitance of the PCB and free-wheel diode: at turn-on, I_D is able to fall before V_{DS} reaches V_{DC} , whilst at turn-off, a capacitive ‘reverse recovery’ overshoot of $I_{D(casc)}$ is evident.

Whilst these effects mean that the switches are not operating under ideal clamped-inductive load conditions, they are representative of the effects found in a real converter and do not significantly affect the comparisons drawn between the different device combinations.

6.3.2.1 Individual devices: Turn-on

In a clamped inductive load, FET turn-on involves I_D rising from zero to I_L , followed by V_{DS} falling from V_{DC} to zero. The rate of rise of I_D is governed by the rate of change of V_{GS} due to V_{ON} , the gate resistance, C_{iss} and g_m [186]. The rate of fall of V_{DS} is determined by the Miller capacitance C_{DG} , gate resistance and difference between the gate drive voltage and plateau voltage $V_{ON} - V_{plat}$.

Of the individual devices, the Si SJ MOSFET has both the slowest current rise and voltage fall. In contrast, the SiC MOSFET has the fastest rise and fall times, with the JFET being somewhere between the two.

Si SJ MOSFET It might appear strange that the Si SJ MOSFET switches slowly compared to the other devices. Its overall turn-on gate resistance, including $R_{GH(LV)}$, gate driver and

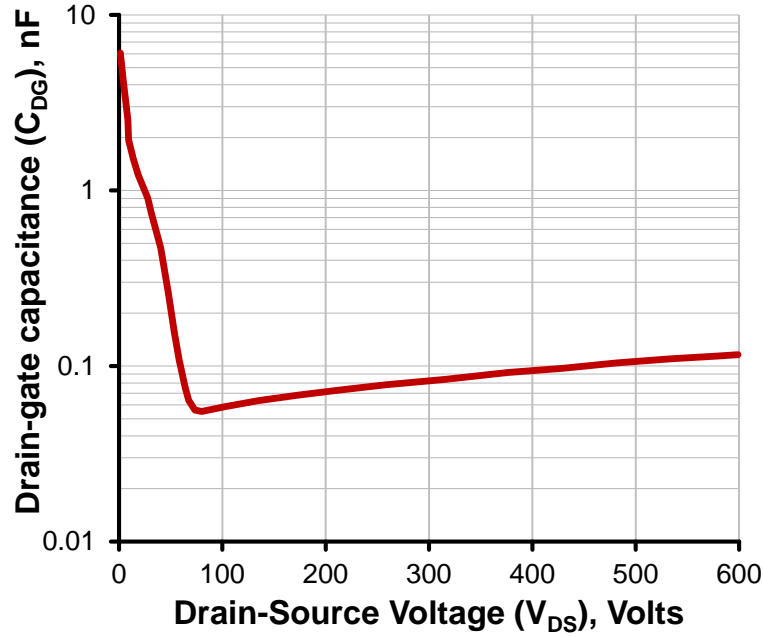


Figure 6.1: Datasheet C_{DG} characteristic for Infineon IPW65R080CFD Si SJ MOSFET [188]

internal resistances, is much smaller than either of the other two devices. It also possesses much higher transconductance than the SiC transistors.

However, it also has an extremely large C_{iss} , whilst the difference between the drive and threshold voltages is the smallest of any of the devices. This leads to a large gate charging time constant, which consequently limits $\frac{dI_D}{dt}$. A faster current rise time would be achievable with a larger V_{ON} , but this would be unusually large.

The slow initial fall of V_{DS} is a curious feature of the extremely non-linear C_{DG} of SJ devices, which initially declines sharply with small, but increasing V_{DS} , before rising again as V_{DS} increases at higher voltages (figure 6.1). Current through a varying capacitance may be expressed as:

$$i = \frac{dQ}{dt} = \frac{d(CV)}{dt} = C \frac{dV}{dt} + V \frac{dC}{dt} \quad (6.1)$$

Therefore, some of the current flowing in the gate resistor R_G that could have contributed to allowing V_{DS} to fall is instead required to allow the magnitude of C_{DG} to change. This can be seen at both turn-on and turn-off in figure 6.2a, where $\left| \frac{dV_{DS}}{dt} \right|$ reaches a maximum at around 100 V, coinciding with the minimum C_{DG} of the device.

SiC MOSFET The SiC MOSFET is notably faster than the other two devices at turn-on. Counter-intuitively, its poor transconductance may actually contribute to its rapid turn-on current rise: the large V_{GS} of at least 20 V required for full enhancement of the channel means

that V_{ON} is substantially bigger than either V_T or the V_{GS} required for rated current to flow. Therefore, despite a larger total gate resistance and lower g_m compared to the other devices, current is able to rise rapidly due to the speed at which V_{GS} rises to a level that can support rated I_D .

The SiC MOSFET experiences a much greater $\frac{dV_{DS}}{dt}$ than the other devices due to the extremely small C_{DG} for this transistor. Even with a comparatively large overall gate resistance and much larger gate driver pull-up resistance, this ensures a small value for the $R_{ON} \cdot C_{DG}$ time constant that limits $\frac{dV_{DS}}{dt}$.

SiC JFET Despite its extremely low C_{iss} , the SiC JFET has a longer current rise time than the SiC MOSFET simply because of a much smaller voltage drop across its otherwise comparable total gate resistance. This leads to a less rapid rise of V_{GS} and hence, despite its superior g_m , a slower increase in I_D . It is not possible to increase V_{ON} significantly to reduce current rise time without causing the gate-source diode to become forward biased and leading to significant gate currents.

Voltage fall is limited by the comparatively high C_{DG} of the JFET, in combination with its high internal gate resistance. This represents a fundamental limit on the turn-on speed of the JFET.

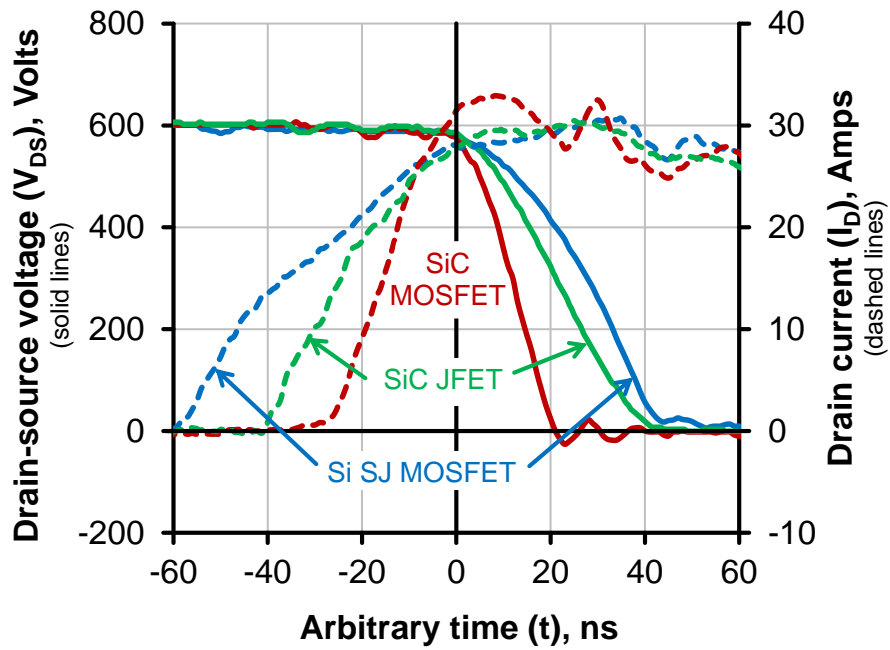
6.3.2.2 Individual devices: Turn-off

FET turn-off performance is largely the inverse of turn-on. The rise of V_{DS} is again limited by C_{DG} , R_{ON} and in this case $V_{plat} - V_{OFF}$. Current fall is determined by the device's forward characteristic as a result of V_{GS} falling due to V_{OFF} , turn-off resistance and C_{iss} .

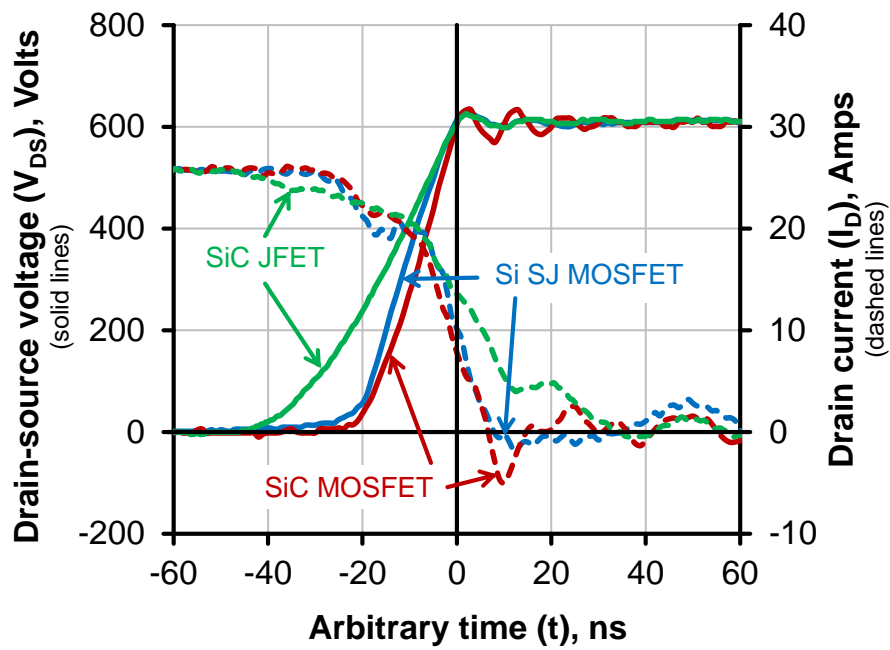
Si SJ MOSFET V_{DS} for the Si devices is able to rise very quickly at turn-off, particularly compared to $\frac{dV_{DS}}{dt}$ at turn on and does so at a similar speed as the SiC MOSFET. This increase in speed may be attributed to the low pull-down resistance of its gate driver which results in around a 30 % lower total gate resistance at turn-off compared to turn-on.

The non-linearity of C_{DG} in this super-junction device is again readily apparent, with a very slow initial rise to several tens of volts, thanks to a low voltage C_{DG} of over 1 nF. V_{DS} then rises very steeply at around 100 V, before reducing in rate as it approaches 600 V and $\frac{dC}{dt}$ effects become significant.

SJ MOSFET $\left| \frac{dI_D}{dt} \right|$ is much greater at turn-off than turn-on and is comparable to both other devices. The large C_{iss} of this device is compensated for by its comparatively high V_T , large transconductance and low total gate resistance at turn-off, resulting in a current fall time equivalent to the SiC MOSFET.



(a) Turn-on



(b) Turn-off

Figure 6.2: Switching characteristics for individual HV transistors. V_{DS} is represented by solid lines and I_D by dashed lines. The Si SJ MOSFET, SiC MOSFET and SiC JFET are represented by blue, red and green lines respectively

SiC MOSFET The rise of V_{DS} at turn-off happens at around the same rate as the fall of V_{DS} at turn-on. This suggests that the significantly lower total gate resistance at turn-off is compensated for by the smaller voltage drop across the gate resistor, leading to a similar Miller current in both cases and a similar $\frac{dV_{DS}}{dt}$ as for the Si SJ MOSFET.

The turn-off current transition is, however, much faster at turn-off than turn-on. This can be attributed to the much smaller internal resistance of the gate driver at turn-off compared to turn-on and this leads to a current fall time similar to that of the Si SJ MOSFET. In this condition, the smaller C_{iss} of the SiC MOSFET compared to the Si SJ MOSFET is more or less entirely compensated for by its lower g_m .

SiC JFET The JFET is again hindered by its comparatively large C_{DG} and $R_{G(int)}$, leading to a voltage rise time of around twice that of the other two devices.

Thanks to the low turn-off resistance and small C_{iss} , I_D initially falls rapidly, at around the same rate as the other devices. However, its fall time is marred by a current 'tail' as I_D drops below around 5 A. This effect is repeatable and was also observed at lower voltages. It becomes less apparent when load current is reduced. Given its apparent dependence on load current, it is likely that this is caused by stray source inductance imposing a voltage that interferes with the usual turn-off process.

6.3.2.3 Individual devices: Summary

The SiC MOSFET generally has superior switching performance compared to the other devices due its extremely rapid switching speeds resulting from its exceptionally low C_{DG} and high drive voltage requirements. However, all the devices have specific drawbacks.

The SiC MOSFET has comparatively onerous drive requirements and operates close to its rated V_{GS} in the on-state. It also suffers from a low V_T . This has the potential to reduce reliability by causing damage to the gate or spurious turn-on due to transients.

The Si SJ MOSFET appears to have excellent characteristics on first inspection and has a turn-off performance comparable to the SiC MOSFET. However it is hampered by its peculiar non-linear C_{DG} and large C_{iss} ; both features of its super-junction design.

The SiC JFET is intrinsically limited by its comparatively large C_{DG} and $R_{G(int)}$ which particularly limit its $\frac{dV_{DS}}{dt}$ capability. In addition, the need to avoid forward biasing its gate-source junction limits the maximum practical turn-on voltage and hence $\frac{dI_D}{dt}$ at turn on. Overall, the SiC JFET has slightly lower switching losses than the SiC SJ MOSFET, but only due to the latter's extremely slow current rise time at turn-on.

Further discussion of switching energies and times is given in section [6.3.3.1](#).

6.3.2.4 Cascode devices: Turn-on

Cascode turn-on is in principle very similar to turn on of a single HV power device. As discussed in section 4.8.1, the LV switch plays little role in the majority of the turn-on process, as it mostly presents only a few milliohms resistance at the source of the HV device. There is one important distinction in the turn-on behaviour of the HV transistor in a cascode circuit however: Rather than being driven by a gate driver, the HV gate is instead supplied from a DC bias voltage, with the change in V_{GS} being effected by the falling source voltage. A HV transistor in the cascode configuration will experience negligible additional ‘gate driver’ impedance.

The choice of gate resistors for a HV transistor in a cascode configuration is likely to be different to those used to control the individual devices as a result of the somewhat different transient behaviour of the cascode. As before, the gate resistances used are given in table 6.1.

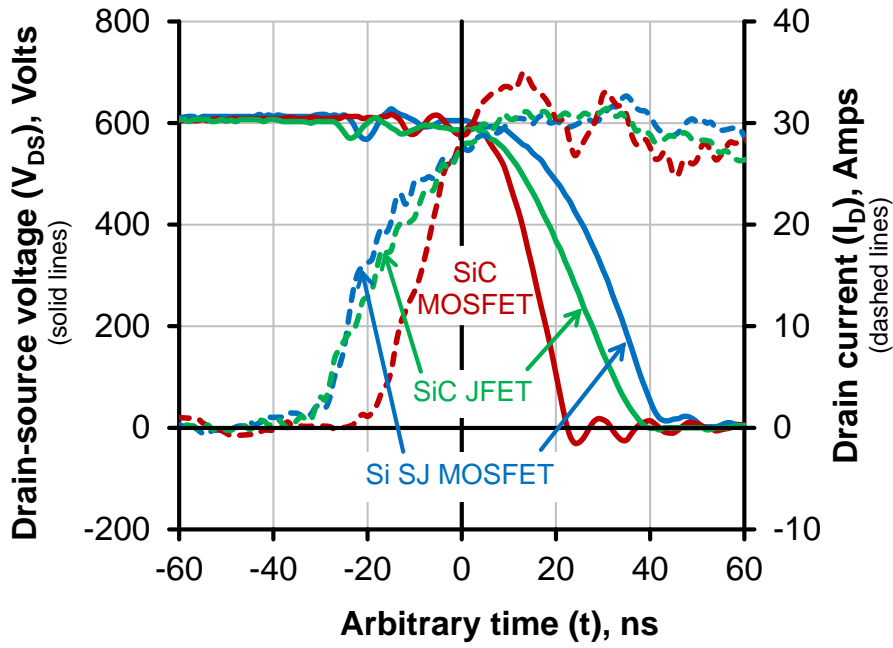
SiC devices There is only a marginal reduction in current rise time for either cascoded SiC device, compared to their individual switching performance. This is because there is a slight reduction in overall gate resistance due to the lack of gate driver gate resistance. However, the effect is small, since it affects only the charging characteristic of C_{iss} . The SiC devices both see a slight reduction in voltage fall time, which may be attributed to the lack of gate driver resistance, particularly in the case of the SiC MOSFET.

Silicon SJ MOSFET There is a large reduction in current rise time for the Si SJ MOSFET, which was found to operate without excessive parasitic oscillation with a much lower HV gate resistance, compared to standalone operation. In conjunction with the absence of gate driver resistance, overall gate resistance for this device is reduced by around 65%, leading to a current rise time comparable to that of the SiC JFET.

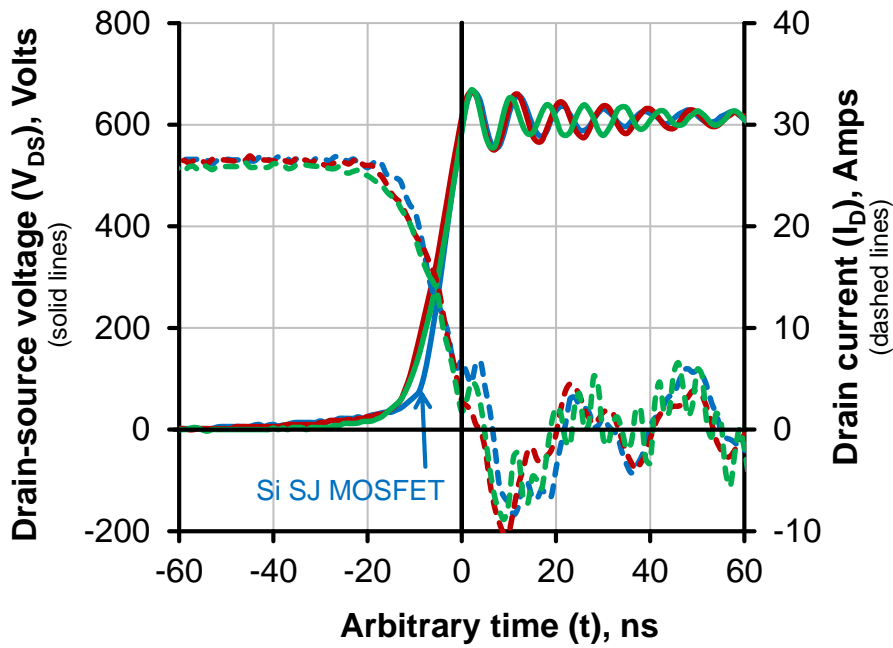
The Si SJ MOSFET also sees an improvement in voltage fall time as a result of the greatly reduced overall gate resistance. However, it is still significantly affected by its non-linear C_{DS} , which again results in its voltage fall time being longer than would otherwise be expected.

6.3.2.5 Cascode devices: Turn-off

As described in section 4.9.2, the cascode turn-off process is markedly different to that of a single transistor. Figure 6.3b shows a slow initial rise of $V_{DS(case)}$ as the drain-source voltage of the LV transistor increases. This dissipates little energy compared to the overall switching process. As $V_{DS(LV)}$ continues to increase, $V_{GS(HV)}$ falls until it reaches its plateau voltage, and begins to turn off, causing $V_{GS(HV)}$ to be held approximately constant. However, the



(a) Turn-on



(b) Turn-off

Figure 6.3: Switching characteristics for cascoded HV transistors. V_{DS} is represented by solid lines and I_D by dashed lines. The Si SJ MOSFET, SiC MOSFET and SiC JFET are represented by blue, red and green lines respectively

continuing rise of $V_{DS(LV)}$ forces increasing Miller current through $R_{G(HV)}$, leading to a very rapid rise of $V_{DS(casc)}$.

The turn off speed of the LV transistor must be approximately matched to that of the HV transistor: If the LV device turns off too quickly, it will experience an excessive $V_{DS(LV)}$ before the HV device is able to start blocking voltage; if it turns off too slowly, it will limit $\frac{dV_{DS(casc)}}{dt}$ and experience significant power dissipation. The most practical way of matching the switching speeds of these two transistors is by selection of an appropriate value of $R_{GL(LV)}$.

This is the reason for the large variation in $R_{GL(LV)}$ required by the different cascode circuits. The Si SJ MOSFET suffers from having a very large $C_{GS(HV)}$, which delays the point at which the HV device blocks voltage and therefore increases $\hat{V}_{DS(LV)}$. Hence the LV device must switch slowly to avoid the large HV gate time constant causing excessive $\hat{V}_{DS(LV)}$ and a disproportionately large value of $R_{GL(LV)}$ is necessary. The much smaller values of $R_{GL(LV)}$ for the two HV SiC devices reflect their much shorter gate time constants as a result of their small $C_{GS(HV)}$.

Similarities between waveforms The need to ensure the switching speeds of the HV and LV devices are well matched leads to a remarkable similarity between the turn-off characteristics for the different devices. For each device combination, the advantages of the HV device are offset by competing requirements of stability and operation within device ratings. For example, the benefit of the low $R_{G(HV)}$ required by the Si SJ MOSFET is offset by its large $C_{GS(HV)}$ and hence large $R_{GL(LV)}$; the benefit of the very low $C_{DG(HV)}$ of the SiC MOSFET is eroded by its necessarily large $R_{GL(LV)}$ and its high gate drive requirement; the benefit of the low $V_{T(HV)}$ of the SiC JFET, is offset by its large $C_{DG(LV)}$ and $R_{G(HV)}$.

Therefore, there is little difference between the turn-off characteristics of any of the device combinations, although it is interesting to note that the effect of the non-linear C_{DG} of the Si SJ MOSFET remains visible.

6.3.2.6 Reliability considerations

Cascode turn-off presents a major problem for the Si SJ MOSFET. In this test, a $\frac{d\hat{V}_{DS}}{dt}$ in excess of 70 GV s^{-1} was measured. This is significantly above the device maximum rating of 50 GV s^{-1} and risks turning on a parasitic BJT inside the device [186]. This would lead to the Si SJ MOSFET becoming uncontrollable, failing in the on-state and being quickly destroyed by excessive current.

It is also not feasible with this device to limit $\frac{d\hat{V}_{DS}}{dt}$ by the use of gate resistors without severely impacting cascode switching performance: increasing $R_{G(HV)}$ would limit $\frac{d\hat{V}_{DS}}{dt}$ for the HV switch, but in doing so would increase the HV gate charging time constant such that

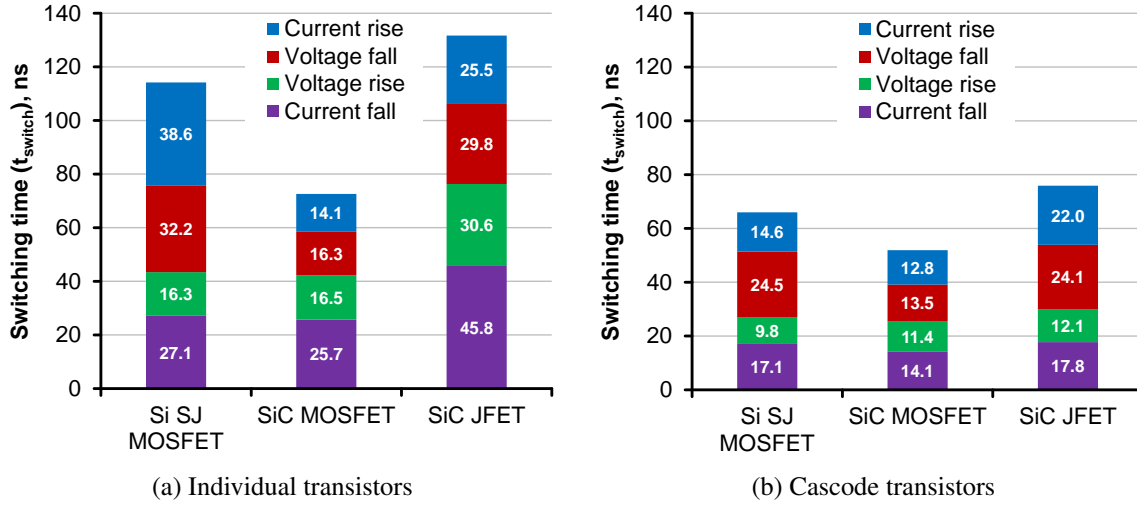


Figure 6.4: Switching times for individual and cascode transistors

the LV switch would experience a catastrophic peak $V_{DS(LV)}$. Increasing $R_{GL(LV)}$ could also limit $\frac{d\hat{V}_{DS}}{dt}$, but only for values of several kilohms. This would lead to excessive turn-off delays of the order of microseconds and a susceptibility to spurious turn-on due to transients.

This problem is specific to the Si SJ MOSFET as a result of its combination of its large C_{iss} and its parasitic BJT. Neither SiC devices is similarly limited: the wide bandgap limits turn-on of the SiC MOSFET parasitic BJT to much higher $\frac{d\hat{V}_{DS}}{dt}$, whilst the SiC JFET has no such parasitic structures. Using such Si SJ MOSFETs in a similar cascode configuration for any practical application is therefore impossible for reliability reasons. However, Si SJ MOSFETs with greater $\frac{dV}{dt}$ immunity are now becoming available and may be suitable for cascode applications in the future [195].

6.3.3 Cascode devices: Conclusion and comparison

The switching times and switching losses for the individual and cascode circuits are compared in figures 6.4 and 6.5 respectively.

6.3.3.1 Performance improvement with cascode configuration

From a switching performance perspective, the use of a cascode circuit to drive HV transistors reduced switching losses by 20 and 35 %, depending on the devices used. It is apparent from both figures 6.4 and 6.5 that much of this improvement comes from reduced turn-off losses, although turn-on performance is still better in each case.

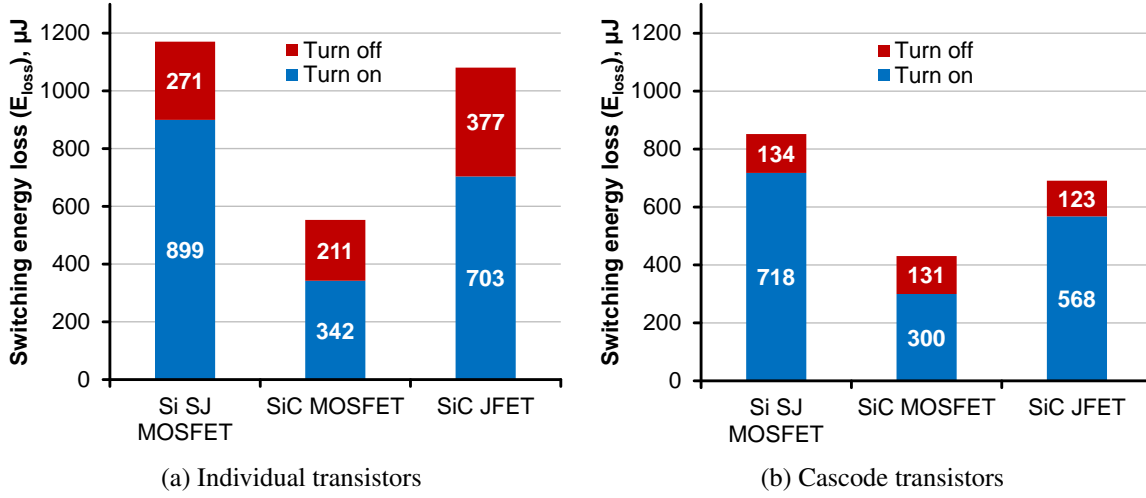


Figure 6.5: Switching losses for individual and cascode transistors

The switching time measurements somewhat over-state this improvement due to the very non-linear switching transients of the Si SJ MOSFET at turn-on and the ‘tail current’ effect in the JFET at turn-off. Reductions in losses at turn-on are as a result of the HV gate bias voltage behaving as a very high quality, low impedance gate driver, leading to faster voltage and current transitions. Reduced turn-off losses are as a result of Miller current being forced to increase as a direct result of rising $V_{DS(LV)}$, leading to very fast voltage rise times.

6.3.3.2 LV switch requirements

The requirements of the LV device are not particularly onerous, provided it has sufficiently highly rated breakdown $V_{DS(LV)}$ to not be damaged by the turn-off voltage peak. A low $R_{DS(ON)}$ helps to minimise additional losses in the on-state and it can also be beneficial for it to have a low inductance package.

6.3.3.3 Cascode drawbacks

The cascode arrangement does have drawbacks that make it unsuitable for use with some HV transistors. In particular, the high turn-off $\frac{dV}{dt}$ it is capable of generating is likely to cause problems in HV devices with a parasitic BJT that could be triggered by switching transients.

It is worth re-iterating that both SiC devices are rated to 1200 V, whilst the Si SJ MOSFET is rated only to 650 V. Since both transistor switching and on-state performance deteriorate with increasing blocking voltage, it is telling that both SiC devices exceed the switching performance of the Si SJ MOSFET, despite being rated to nearly twice the blocking voltage.

6.3.3.4 Dubious manufacturer's claims

The overall switching energy measurements for the SiC JFET are particularly interesting, as the 1081 μJ measured at 600 V and 25 A is substantially higher than the 290 μJ at 600 V and 17 A listed in the device datasheet [79]. Even making the same measurement at 600 V and 17 A yielded a switching energy 632 μJ : over twice the stated value. This is due to the gate drive levels chosen.

In these experiments, the gate was switched between -10 and +2.5 V to ensure that the maximum gate voltage of -15 V was not exceeded by turn-off transients and to ensure that the gate-source diode does not become forward biased at around +2.6 V. However, the switching energies quoted in the device datasheet are for switching between the rated gate-source voltages of -15 and +15 V. This approach gives unrealistically low switching energies.

Operating SiC JFETs in this manner in any practical converter will cause significant problems with reliability, since switching transients are likely to cause the rated gate voltages to be regularly exceeded at both turn-on and turn-off. In the on-state, the heavily forward biased gate diode will cause excessive power dissipation in both the JFET and the gate resistor of the order of many tens of watts. Thus, any reductions in energy losses due to lower switching energies would be overwhelmed by the greatly increased on-state power losses.

6.4 Gate resistance control of cascode circuits

As has been shown in the preceding section, the appropriate matching of HV and LV transistor switching speeds is essential for proper operation of cascode circuits. Under most circumstances, this can easily be achieved by the selection of gate resistances for the HV and LV devices. The equations developed in the simplified model of chapter 4 are helpful for understanding the effect of gate resistance, but must be verified using experimental measurements.

A series of experiments of clamped-inductive cascode switching with different gate resistances was therefore undertaken to examine the effects of gate resistance on cascode switching.

For these experiments, a cascode constructed from a PCB mounted SJP120R085 SiC JFET die and an EPC2015 eGaN FET was used. This very low inductance arrangement was used to ensure that the effects of gate resistance were dominant compared to PCB strays. Due to the sensitivity of the LV eGaN FET gate to over-voltages, a turn-on voltage of 4.1 V was used. However, the high gain of this part ensured that its switching behaviour was not unduly influenced by the comparatively low gate drive voltage.

The turn-on and turn-off waveforms of the cascode circuits were compared for different values of gate resistance. At turn-on, the values of $R_{G(HV)}$ and $R_{GH(LV)}$ were varied over a range of 1.5 to 6.8 Ω and 1.0 to 100 Ω respectively. $R_{GL(LV)}$ plays no part in turn-on, so was

not considered. At turn-off, the values of $R_{G(HV)}$ and $R_{GL(LV)}$ were varied over a range of 1.5 to 6.8 Ω and 10 to 470 Ω respectively. $R_{GH(LV)}$ plays no part in turn-off, so was not considered.

In all cases, the waveforms of $V_{DS(casc)}$, $I_{D(casc)}$, $V_{DS(LV)}$, $V_{GS(HV)}$ and $V_{GS(LV)}$ were measured. This made it possible to investigate the effects of gate resistance on the switching stresses experienced by both devices, rather than simply the drain currents and voltages. It is important to note that the measurement of $V_{GS(HV)}$ was calculated as the difference between the $V_{G(HV)}$ and $V_{DS(LV)}$. As discussed previously in section, 4.6.1.3 it does not include the effects of either the JFET internal gate resistance or any stray inductance between the HV source and LV and this measurement must therefore be treated with some caution.

6.4.1 Effect of $R_{G(HV)}$

Since $R_{G(HV)}$ is an intrinsic part of the HV gate circuit, its value affects both the turn-on and turn-off switching processes. Turn-on and turn-off waveforms in which $R_{G(HV)}$ is increased from 1.5 to 6.8 Ω are shown in figures 6.6 and 6.7.

6.4.1.1 Turn-on

At turn-on, increasing the size of $R_{G(HV)}$ limits turn-on $\frac{dV_{DS(casc)}}{dt}$ by increasing the fall time of $V_{DS(casc)}$. There is not a linear relationship between the decrease in $\left| \frac{dV_{DS(casc)}}{dt} \right|$ and the fall time of $V_{DS(casc)}$, with behaviour becoming increasingly non-linear at lower voltages as $R_{G(HV)}$ increases. This means that increasing $R_{G(HV)}$ could be used as a method of limiting $\frac{dV_{DS(casc)}}{dt}$, but would also incur disproportionate turn-on losses, particularly for larger values.

Increasing $R_{G(HV)}$ has no effect on the rate of rise of $I_{D(casc)}$. However, larger values do show a clear damping effect on the HV gate circuit. Some parasitic oscillation is visible in the $V_{DS(LV)}$, $V_{GS(HV)}$ and $V_{GS(LV)}$ waveforms, due to the very rapid initial fall of $V_{DS(LV)}$ (see section 4.9.1). The severity of this oscillation is reduced by increasing the magnitude of $R_{G(HV)}$, suggesting that this gate resistance has an important role to play in ensuring stability of the cascode at turn-on, if not in controlling $V_{DS(casc)}$ or $I_{D(casc)}$. As will be shown in section 6.5, these parasitic oscillations may also be controlled by increasing $L_{S(HV)}$.

The turn-on behaviour dependence on $R_{G(HV)}$ reflects that predicted by the simplified equations derived in section 4.10, as it only has a significant specific effect on the $V_{DS(casc)}$ and $V_{GS(HV)}$ waveforms. However, the increasingly non-linear fall of $V_{DS(casc)}$ with increasing $R_{G(HV)}$ shows that the simplified model starts to reach its limits once $R_{G(HV)}$ becomes sufficiently large to significantly affect the fall time of $V_{DS(casc)}$.

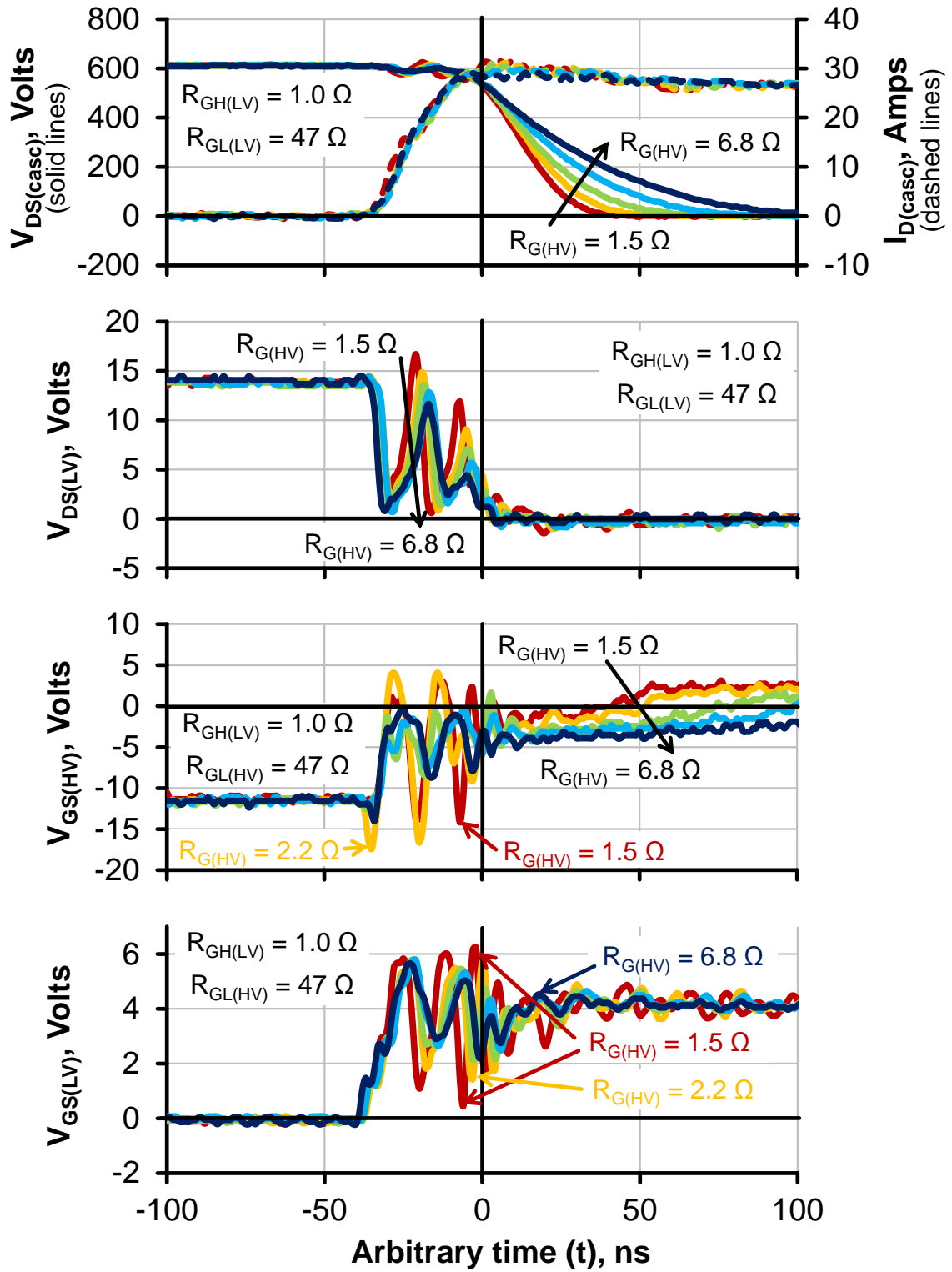


Figure 6.6: Turn-on waveforms for $R_{G(HV)} = 1.5, 2.2, 3.3, 4.7$ and 6.8Ω . $R_{GH(LV)}$ and $R_{GL(LV)}$ are held constant at 1.0Ω and 47Ω respectively.

6.4.1.2 Turn-off

The feasible range of values of $R_{G(HV)}$ is set by its effect on cascode turn-off behaviour. As $R_{G(HV)}$ increases, it causes the HV device to both respond more slowly to the changing value of $V_{DS(LV)}$ and then to turn-off more slowly once $V_{GS(HV)}$ reaches its turn-off plateau. This means that $V_{DS(LV)}$ increases over a longer period of time and is required to block a greater proportion of $V_{DS(casc)}$.

Larger values of $R_{G(HV)}$ therefore mean that $V_{DS(LV)}$ rises faster and for longer before $I_{D(casc)}$ falls, resulting in larger peak values of $V_{DS(LV)}$. This sets a limit on the maximum value of $V_{G(HV)}$. If it is too large, the voltage rating of the LV switch will be exceeded, with negative implications for the efficiency and reliability of the switch.

In common with the turn-on waveforms, $R_{G(HV)}$ has no influence over the current waveforms for the range of values investigated. However, unlike the turn-on case, it also has only a small effect on $V_{DS(casc)}$ waveform. This is due to the effect of $R_{G(HV)}$ on $V_{DS(LV)}$ discussed previously. The larger values of $V_{DS(LV)}$ associated with larger $R_{G(HV)}$ also increase the voltage across $R_{G(HV)}$, causing a larger Miller current to flow than would otherwise be possible. There is therefore only a weak relationship between increasing $R_{G(HV)}$ and increasing turn-off $V_{DS(casc)}$ rise time.

In a similar manner to the turn-on case, Increasing $R_{G(HV)}$ also helps to damp the response of the HV gate circuit. This is particularly clear in the $V_{GS(HV)}$ and $V_{GS(LV)}$ waveforms, where larger values ensure better damping of parasitic oscillations. These experimental measurements are generally reflected in the predictions of the simplified model. However, the slight dependence of current fall on $R_{G(HV)}$ predicted by the equations is not apparent, due to the imperfect nature of the clamped inductive load arising from the stray drain-source and free-wheel diode parasitic capacitance.

6.4.2 Effect of $R_{GH(LV)}$

The effect of increasing the $R_{GH(LV)}$ on cascode turn-on waveforms is shown in figure 6.8. As predicted by the linearised model, its value affects all turn-on waveforms. Unlike $R_{G(HV)}$, $R_{GH(LV)}$ is able to control both the rise-time of $I_{D(casc)}$ and the fall time of $V_{GS(casc)}$ when large values are used, although it is noticeably more effective at limiting $\frac{dI_{D(casc)}}{dt}$ than $\frac{dV_{DS(casc)}}{dt}$. Whilst this does provide a method of controlling turn on $\frac{dV_{DS(casc)}}{dt}$ and $\frac{dI_{D(casc)}}{dt}$, $R_{GH(LV)}$ cannot control these parameters independently, resulting in excessive switching losses if it is only necessary that one is limited.

The control of turn on $\frac{dV_{DS(casc)}}{dt}$ and $\frac{dI_{D(casc)}}{dt}$ by $R_{GH(LV)}$ is not predicted by the linearised equations. This arises intentionally, due to the assumption in the simplified model that the LV

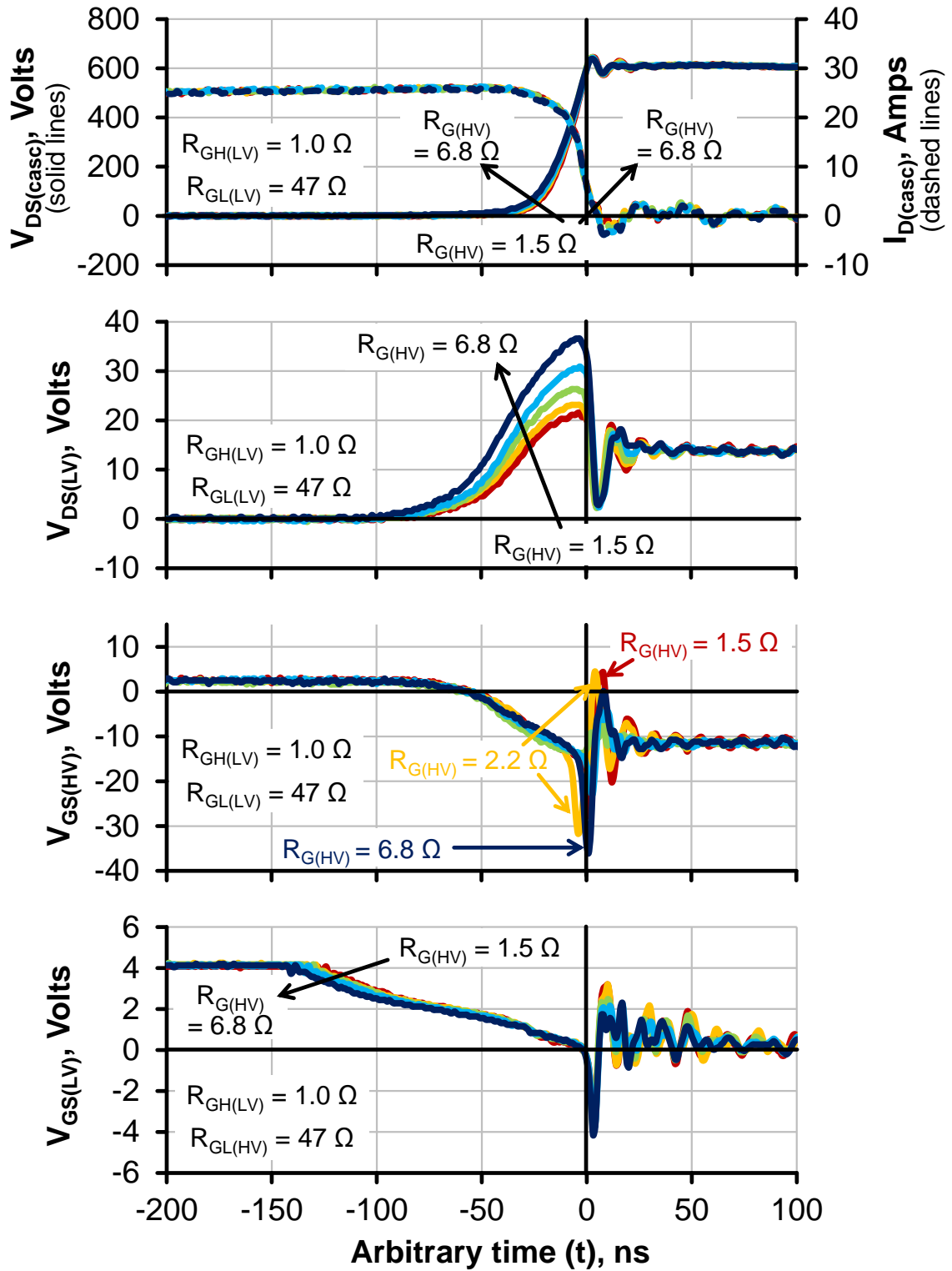


Figure 6.7: Turn-off waveforms for $R_{G(HV)} = 1.5, 2.2, 3.3, 4.7$ and 6.8Ω . $R_{GH(LV)}$ and $R_{GL(LV)}$ are held constant at 1.0Ω and 47Ω respectively.

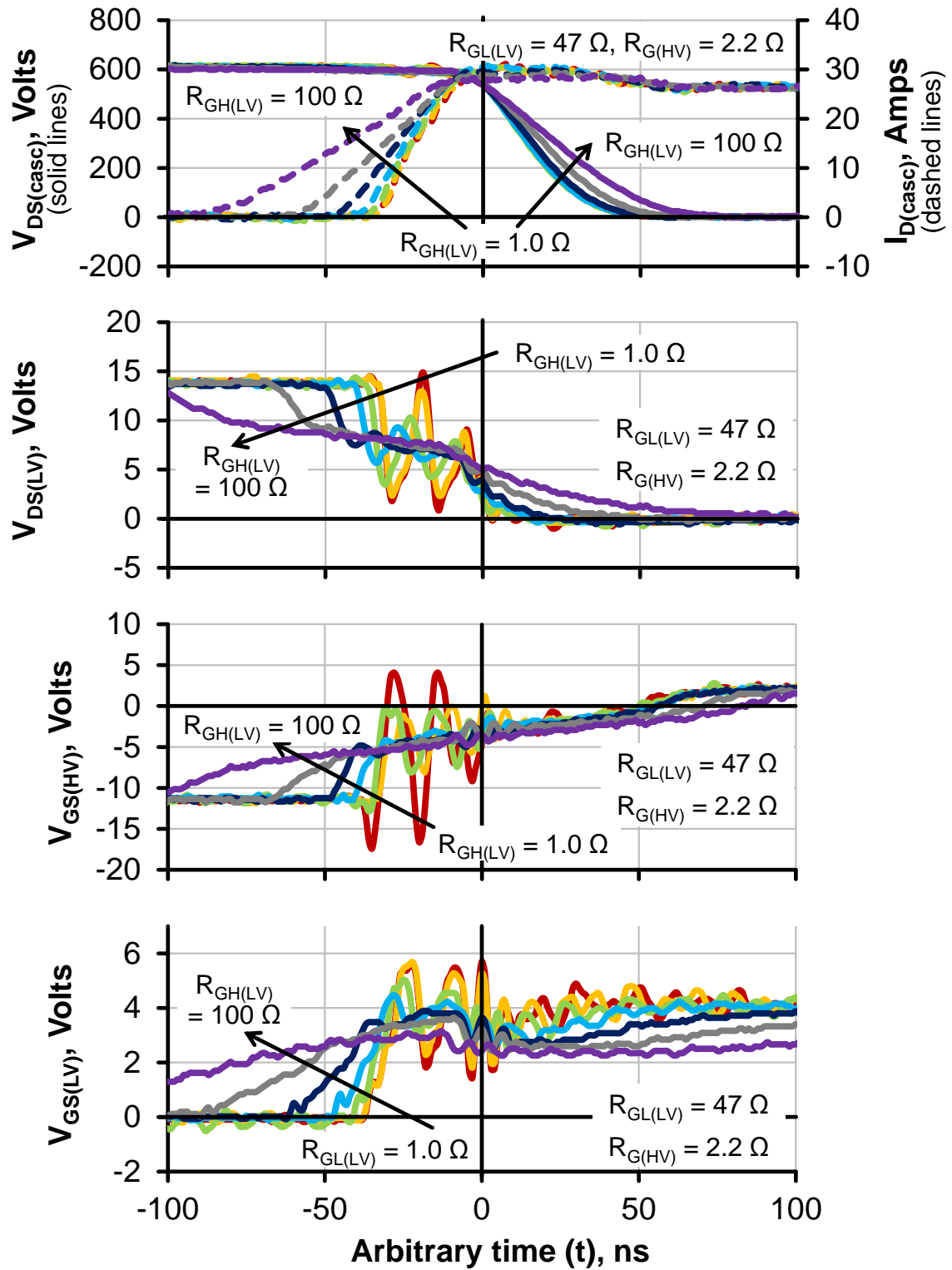


Figure 6.8: Turn-on waveforms for $R_{GH(LV)} = 1, 2.2, 4.7, 10, 22, 47$ and 100Ω . $R_{GL(LV)}$ and $R_{G(HV)}$ are held constant at 47Ω and 2.2Ω respectively.

switch turns on extremely quickly, both for reasons of efficiency and because turn-on switching transients are rarely as severe as those of turn-off. Siemieniec et al. have suggested using large values of $R_{GH(LV)}$ to control these transients [141]. However, this mode of operation is very different to that in which the LV transistor is switched on as quickly as possible, with this device instead remaining in its saturation region for much of the switching process. From the work presented in this thesis, other approaches such as increasing $C_{DG(HV)}$ or $L_{S(HV)}$ are likely to provide more effective control of these transients.

An effect of particular note in figure 6.8 is the beneficial effect of $R_{G(HV)}$ on the overall stability of the cascode. In this case there is a clear optimum value of $R_{GH(LV)}$ of $10\ \Omega$, at which the rise time of $I_{D(casc)}$ and the fall time of $V_{DS(casc)}$ are close to the minimum values, but with minimal parasitic oscillations. Larger values of $R_{GH(LV)}$ switch unnecessarily slowly with little improvement in stability, whilst smaller values lead to excessive ringing with no improvement in switching response. This suggests that optimising the choice of $R_{GH(LV)}$ in cascode circuits is an important consideration for best performance.

One apparent discrepancy between the measurements in figure 6.8 and the models of cascode operation is the plateau in $V_{DS(LV)}$ that occurs as $I_{D(casc)}$ rises. This is due to the source inductance of the LV transistor ($L_{S(LV)}$) being of a similar order to the very low $L_{S(HV)}$ of the PCB. As $I_{D(casc)}$ rises, the voltage imposed across $L_{S(LV)}$ prevents $V_{DS(LV)}$ falling to zero. Despite the differences between model predictions and measurements of $V_{DS(LV)}$ during this period, this effect has little influence on the accuracy of model predictions of other waveforms, since $L_{S(LV)}$ can readily be combined with that of $L_{S(HV)}$ to form a single lumped inductance between the two transistors. Additionally, in a large proportion of practical circuits, the magnitude of $L_{S(HV)}$ is likely to be sufficiently large compared to $L_{S(LV)}$ that this effect will be negligible.

6.4.3 Effect of $R_{GL(LV)}$

The effect of increasing the $R_{GL(LV)}$ on cascode turn-off waveforms is shown in figure 6.9. This is primarily useful as a method of limiting $\frac{dV_{DS(casc)}}{dt}$. It can clearly be seen from this diagram that whilst increasing $R_{GL(LV)}$ does indeed constrain the rate of rise of $V_{DS(casc)}$, very large values are required to have a significant impact, due to the non-linear rise in $V_{DS(casc)}$. Such large values also severely limit the rate of change of the gate waveforms of the HV and LV devices as well as $V_{DS(LV)}$, leading to excessive switching delays of the order of hundreds of nanoseconds.

Large values of $R_{GL(LV)}$ also lead to an unusual effect as the $I_{D(casc)}$ falls, with a ‘tail current’ effect being visible for values of $R_{GL(LV)}$ in excess of $100\ \Omega$. This is due to a second-

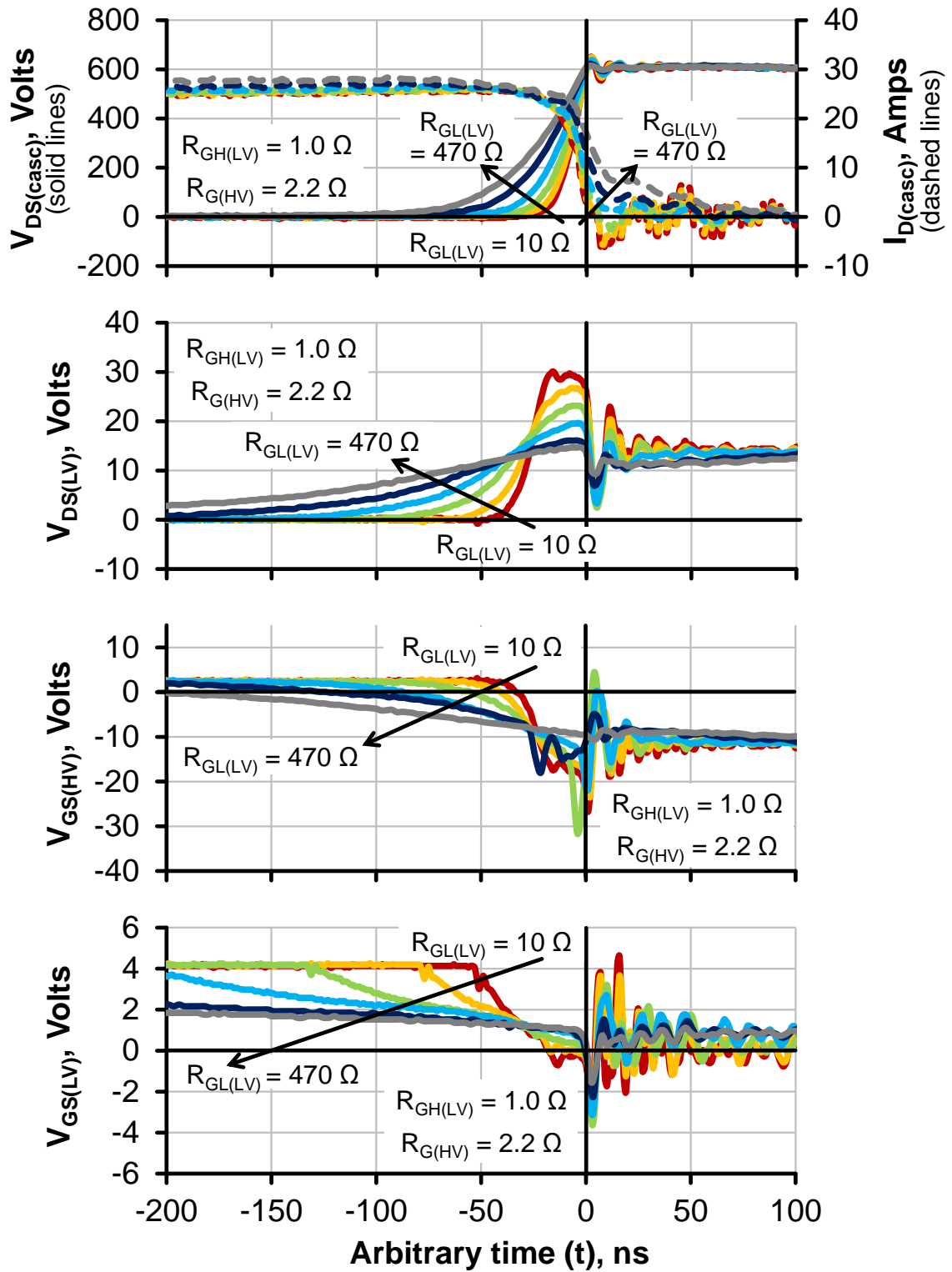


Figure 6.9: Turn-off waveforms for $R_{GL(LV)} = 10, 22, 47, 100, 220$ and 470Ω . $R_{GH(LV)}$ and $R_{G(HV)}$ are held constant at 1.0Ω and 2.2Ω respectively.

order effect that arises from the redistribution of charge that occurs as $I_{D(casc)}$ falls, previously described in section 4.9.2. As the value of $V_{DS(LV)}$ falls rapidly as a result of this process, a displacement current flows through $C_{DG(LV)}$ to charge $C_{iss(LV)}$. When $R_{GL(LV)}$ is large, this prevents the LV transistor turning off fully until this additional charge is able to flow out of the LV gate through $R_{GL(LV)}$.

This ‘tail current’ effect is unusually prominent in these measurements due to the extremely low threshold voltage and high gain of the EPC2015 LV transistor. This effect is not predicted by the simplified cascode model, because the charge redistribution effect is modelled as instantaneous and effects on the LV gate are not considered. Moreover, in reality charge redistribution occurs over a proportion of the current fall period, rather than just at the end, as assumed in the simplified model. However, since this effect is only of concern for very large $R_{GL(LV)}$, this is unlikely to cause serious problems in practical circuits and alternative methods are preferred for significant $\frac{dV_{DS(casc)}}{dt}$ limiting (section 6.6).

As with the other gate resistors, $R_{GL(LV)}$ has a clear influence on controlling parasitic oscillations, with larger values generally leading to smaller oscillations. Its size also has a role to play in limiting the peak value of $V_{DS(LV)}$ by limiting the switching speed and hence voltage rise of the LV transistor. In practice this means its value should therefore be selected in conjunction with that of $R_{G(HV)}$. However, as the measurements of figure 6.9 show, the use of large values is likely to cause undesirable consequences including substantial turn-off delays and excessive switching losses.

6.4.4 Gate resistances: summary

The choice of gate resistance in a cascode switch can be critical for ensuring well-controlled, optimised switching. In particular, proper selection of the $R_{G(HV)}$ and $R_{GL(LV)}$ gate resistors is important to ensure that the switching speeds of the HV and LV devices are matched at turn-off to avoid damaging values of $V_{DS(LV)}$. This requires a trade-off between limiting $V_{DS(LV)}$ to reasonable values and avoiding excessive switching losses.

Optimising the selection of these gate resistors can be assisted by the use of simulation. Figure 6.10 represents the peak $V_{DS(LV)}$ vs. turn-off energy losses over a wide range of values of $R_{G(HV)}$ and $R_{GL(LV)}$, based on SPICE simulation of the cascode circuit described in section 4.11. This simulation shows a good match with the experimental results described previously and clearly shows the need for comparatively large values of $R_{GL(LV)}$ and small values of $R_{G(HV)}$ to limit $V_{DS(LV)}$ without greatly increasing turn-off losses. Most importantly, this shows that the values of $R_{G(HV)}$ and $R_{GL(LV)}$ must ensure that HV and LV device switching speeds are well-matched, to optimise the trade-off between switching losses and $\hat{V}_{DS(LV)}$.

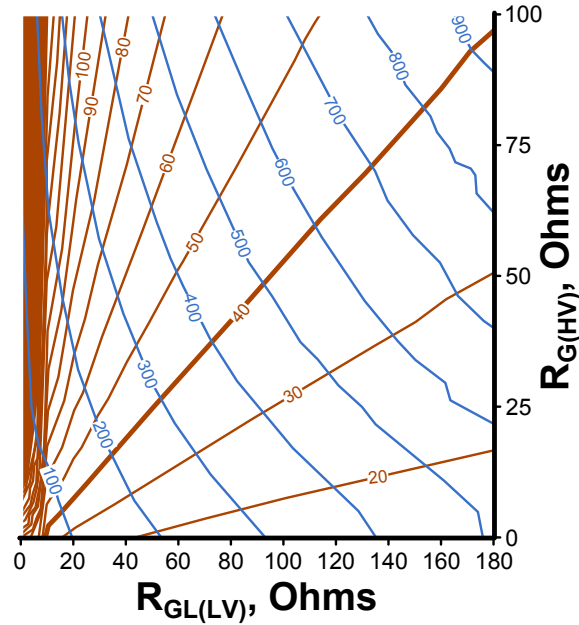


Figure 6.10: Contour plot showing trade-off between $V_{DS(LV)}$ in Volts (red lines) vs. turn-off energy loss in μJ (blue lines) for various values of $R_{GL(LV)}$ and $R_{G(HV)}$. The rated $V_{DS(LV)}$ of the LV transistor is represented by the thick red line.

Gate resistors also have an important role to play in damping parasitic oscillations during switching and optimum values can be found that minimise switching losses without sacrificing stability.

It is also possible to gain a degree of control over the $V_{DS(casc)}$ and $I_{D(casc)}$ switching transients. However, from experimental evidence it is clear that gate resistor selection is not a sophisticated method of controlling these transients and that it is difficult to avoid affecting both the voltage and current waveforms by doing so. In addition, substantially limiting cascode switching speed causes excessive switching delays which are likely to be undesirable in a practical converter, particularly if turn-on and turn-off delays are asymmetric.

6.5 Effect of stray inductance on cascode circuits

Stray inductance is an inevitable feature of practical cascode circuits. Understanding the sensitivity of the cascode circuits to the presence of stray inductance in different locations is therefore important for optimising their layout.

The same experimental set-up described in the previous section was used to investigate the effect of varying the stray inductance in different locations of the circuit. Commercially characterised surface mount air core inductors with nominal inductances of 2.5, 5.0, 8.0, 12.5

and 18.5 nH were used to add extra inductance to the circuit at several locations, as described in section 3.8.

Additional inductance was included at the drain, gate and source of the HV device. Additional inductance was not included at the gate and source of the LV transistor due to the impracticality of doing so, due to the extremely small package of the LV transistor and its very short gate and source PCB traces. In any case, as long as the gate driver ground reference is provided via a Kelvin connection directly to the LV transistor source, the effect of any stray source inductance can be eliminated. Additionally, in most practical cascodes, the HV device is likely to be packaged in such a way that its source inductance is large in comparison to that of the LV source inductance.

The turn-on and turn-off waveforms of the cascode circuits were compared for different values of additional inductance at the locations described. In all cases gate resistors of $R_{G(HV)} = 2.2 \Omega$, $R_{GH(LV)} = 4.7 \Omega$ and $R_{GL(LV)} = 47 \Omega$ were used to give reasonably controlled, but rapid switching. The maximum size of inductances investigated was limited by their detrimental effect on switching, with values larger than 18.5 nH causing several device ratings to be exceeded.

6.5.1 Effect of HV gate and drain inductance

Although measurements of the effects of stray inductance at the HV drain, gate and source were taken, only the addition of inductance to the HV source was found to have a substantial effect on $I_{D(casc)}$ or $V_{DS(casc)}$ over the range of 0 - 18.5 nH. Increasing the inductance at the gate and drain of the HV did increase the susceptibility of the cascode to parasitic oscillations, with the gate being more sensitive to this effect. Indeed the addition of gate inductance had a sufficiently large effect on parasitic oscillations that the maximum practical additional inductance was limited to 12.5 nH to avoid significantly exceeding the LV $V_{GS(LV)}$ rating.

Minimising inductance at the HV gate or drain is therefore helpful to minimise parasitic oscillations, but has little effect on switching speed. Due to the limited effect of these inductances on switching transients, the waveforms for these experiments are not reproduced here and may instead be found in appendix E.

6.5.2 Effect of HV source inductance, $L_{S(HV)}$

The size of the HV source inductance, $L_{S(HV)}$ has an important influence at both turn-on and turn-off. This is shown respectively in figures 6.11 and 6.12.

At turn-on, the magnitude of $L_{S(HV)}$ directly determines the rate of rise of $I_{D(casc)}$ and provides a straightforward method of controlling this process. There is a slight increase in

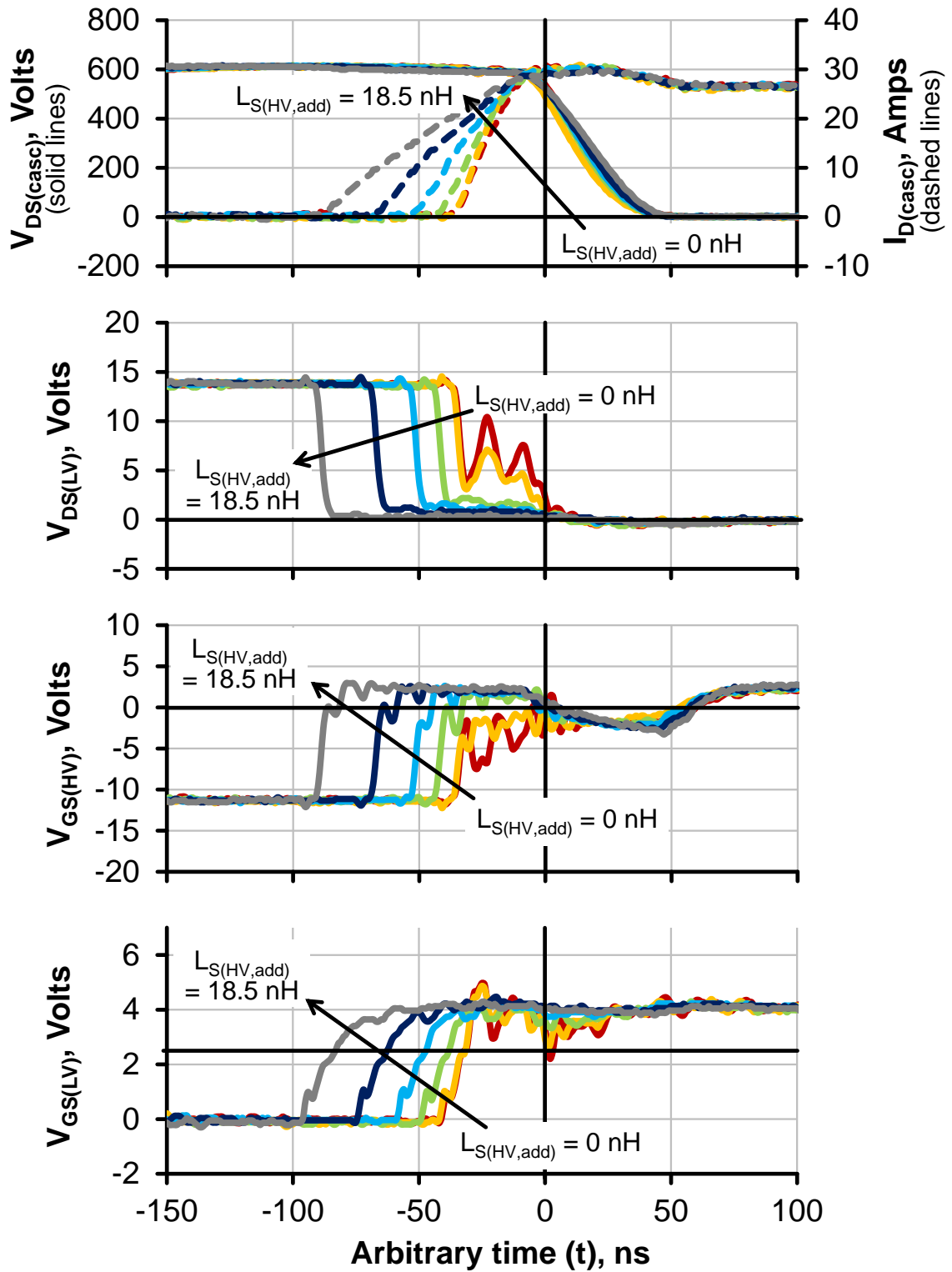


Figure 6.11: Turn-on waveforms for $L_{S,add} = 0, 2.5, 5, 8, 12.5$ and 18.5 nH with $R_{G(HV)} = 2.2 \text{ } \Omega$, $R_{GH(LV)} = 4.7 \text{ } \Omega$ and $R_{GL(LV)} = 47 \text{ } \Omega$

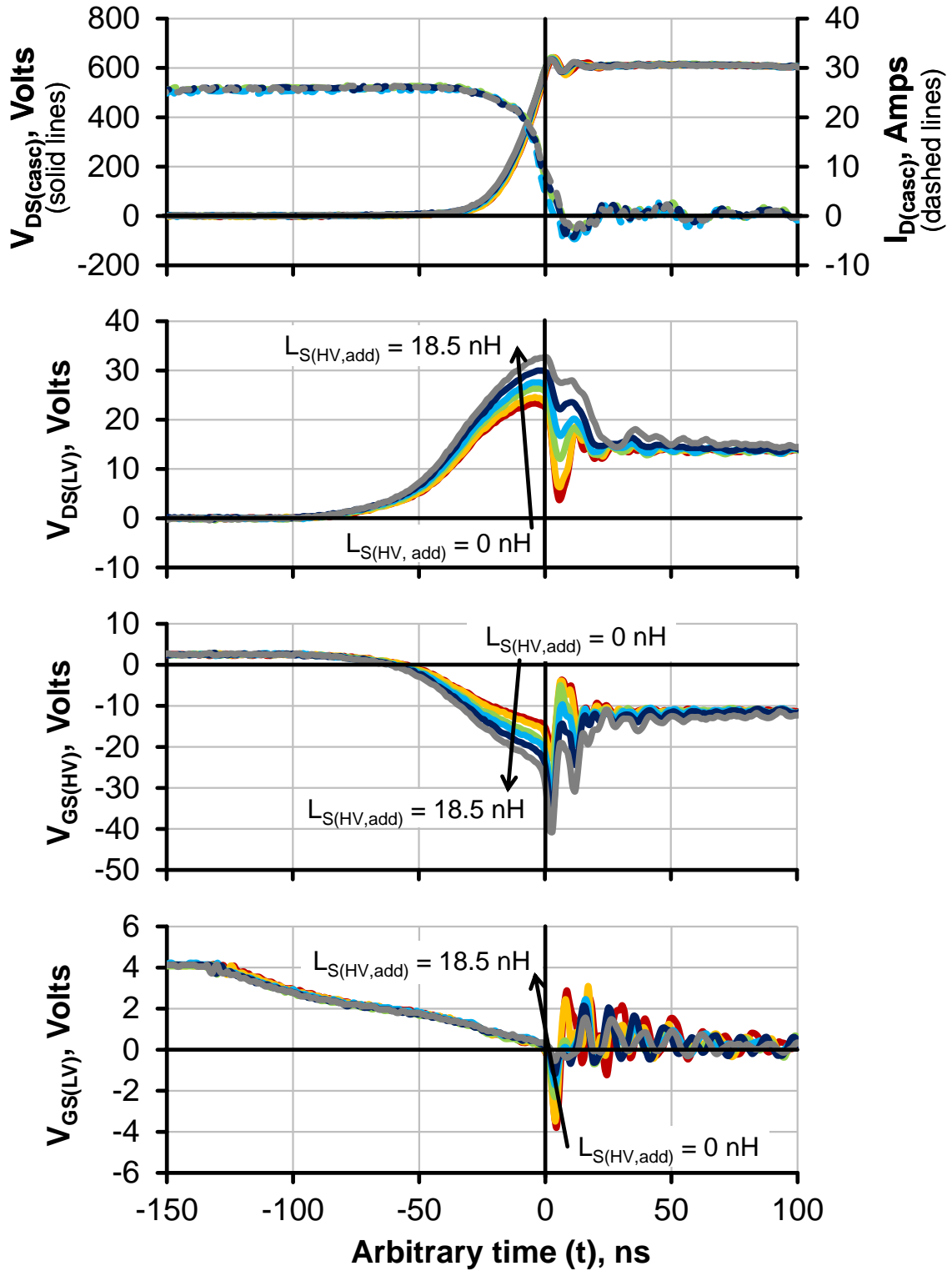


Figure 6.12: Turn-off waveforms for $L_{S,add} = 0, 2.5, 5, 8, 12.5$ and 18.5 nH with $R_{G(HV)} = 2.2 \Omega$, $R_{GH(LV)} = 4.7 \Omega$ and $R_{GL(LV)} = 47 \Omega$

voltage fall time with rising $L_{S(HV)}$, but this effect is small compared to its effect on current. A non-zero value of $L_{S(HV)}$ had a beneficial effect on turn-on stability. This can be seen very clearly in 6.11, where the addition of 5 nH of inductance at the HV source has a negligible effect on the $I_{D(casc)}$ and $V_{DS(casc)}$ but a large effect in reducing the parasitic oscillations visible in the other waveforms.

The effect of $L_{S(HV)}$ at turn-off is somewhat different to the turn-on case. Larger values of $L_{S(HV)}$ slightly decrease the rate of rise of $V_{DS(casc)}$, since the voltage developed across this stray inductance during this stage of switching becomes more significant and slightly reduces the Miller current through $R_{G(HV)}$. This effect, in conjunction with the slight delaying effect larger values of $L_{S(HV)}$ have on the HV gate circuit, causes $V_{DS(LV)}$ to rise to a higher peak value over the period in which $V_{DS(casc)}$ rises.

It might be expected that increasing $L_{S(HV)}$ would significantly reduce turn-off $\frac{dI_{D(casc)}}{dt}$, but this is not the case, as can be seen in the $V_{DS(LV)}$ waveform of figure 6.12, $\hat{V}_{DS(LV)}$ is critical for determining the voltage that is imposed across the stray inductance as $I_{D(casc)}$ falls. As a result, larger values of $L_{S(HV)}$ also experience a larger negative voltage during the current fall stage and hence there is negligible effect on the fall time of $I_{D(casc)}$.

This effect is not considered in the simplified model, due to the assumption that the voltage across $L_{S(HV)}$ remains small during whilst $V_{DS(casc)}$ rises. However, this does not cause serious problems with the accuracy of the basic predictions of the model, since turn-off $V_{DS(casc)}$ and $I_{D(casc)}$ are largely unaffected by additional $L_{S(HV)}$. Furthermore, the peak value of $V_{DS(LV)}$ is within 20% of the no additional inductance case, even with 8 nH of additional inductance. This would be a large value of stray inductance in a practical circuit and lends confidence that the simplified model is not unduly sensitive to stray inductance effects.

6.5.3 Stray inductance conclusions

This experimental work has investigated the effects of stray inductance on cascode switching performance and provides an insight into how layout can be optimised. The presence of stray inductance at the gate or source of the HV device has no discernable effect on switching losses, although its value should be minimised where possible to avoid excessive parasitic oscillations during switching. In particular, parasitic ringing due to HV gate inductance can also lead to substantial voltage oscillations at the LV gate.

$L_{S(HV)}$ does influence switching behaviour, although its effects at turn-on and turn-off are markedly different. Since increasing $L_{S(HV)}$ is only able to significantly limit $\frac{dI_{D(casc)}}{dt}$ at turn-on, there is no practical method of limiting turn-off $\frac{dI_{D(casc)}}{dt}$ by selection of gate resistors or by the addition of stray inductance. By inspection of the simplified model, the only practical

method for limiting turn-off $\frac{dI_{D(casc)}}{dt}$ is therefore by selection of V_{bias} and $V_{T(HV)}$ to minimise the voltage imposed across $L_{S(HV)}$ at turn-off. This finding corroborates the concept patented by Bhalla for increasing turn-on $\frac{dI_D}{dt}$ [120].

Non-zero values of $L_{S(HV)}$ are not necessarily detrimental to cascode operation and small values even contribute to turn-on stability, in conjunction with a suitable choice of $R_{GH(LV)}$. However large values of $L_{S(HV)}$ lead to unnecessarily large $\hat{V}_{DS(LV)}$, which can be detrimental for the reliability of the cascode, due to the increased voltage stresses on the LV transistor.

For a given layout, it is preferable to increase cascode drain or gate inductance to reduce either $L_{S(HV)}$ or LV source inductance to their optimum levels. This corroborates the earlier findings from simulation work presented in [185].

6.6 Control of $\frac{dV}{dt}$ transients

The control of voltage transients is important in applications where EMI is a concern. The effect of gate resistors on both voltage and current transients has already been investigated in section 6.4. However, this showed that whilst controlling both turn-on and turn-off $\frac{dV}{dt}$ using gate resistances is possible, there are several practical limitations to this technique.

6.6.1 Control of $\frac{dV}{dt}$ by Aggeler's method

Techniques for controlling cascode $\frac{dV}{dt}$ were studied by Aggeler et al. [142] with early SiC JFETs, over a limited current and voltage range. Two techniques were proposed: the inclusion of additional capacitance, C_A , between the drain of the HV switch and the gate of the LV switch (method A) and the inclusion of additional capacitance, C_B , between the drain and gate of the HV switch (method B). The two methods are shown in figure 6.13.

To determine whether the techniques proposed by Aggeler et al. are still applicable for a cascode of higher voltage and current rating, the effect of adding capacitance to control $\frac{dV_{DS(casc)}}{dt}$ in this manner was investigated experimentally using the same SiC MOSFET cascode described previously. Similar gate resistances of $R_{GL(LV)} = 3.3 \Omega$, $R_{GH(LV)} = 3.3 \Omega$ and $R_{G(HV)} = 4.7 \Omega$ to ensure a rapid switching speed with no additional capacitance. The exceptionally high $\frac{dV}{dt}$ capability of this circuit makes it an attractive candidate for studying $\frac{dV}{dt}$ control, whilst its high power rating significantly expands on the scope of the previous study.

6.6.1.1 Method A: additional capacitance between HV drain and LV gate (C_A)

The effect of adding capacitance between the HV SiC MOSFET drain and LV MOSFET gate is shown in figure 6.15. The additional values used were 16.5, 33, 66 and 100 pF.

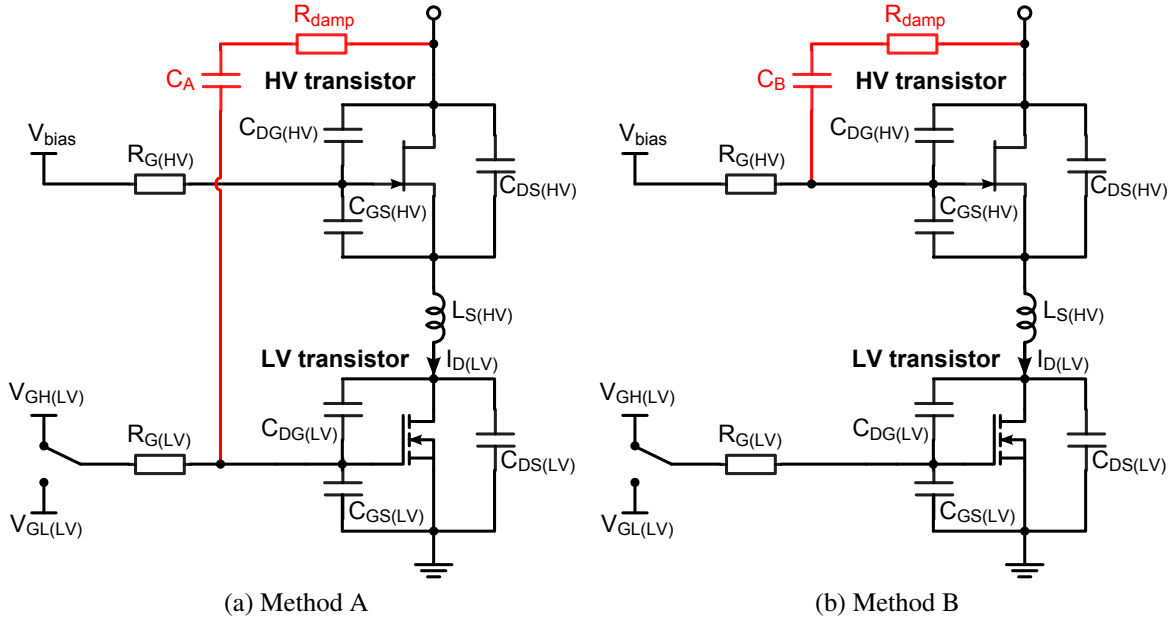


Figure 6.13: $\frac{dV}{dt}$ control methods originally proposed by Aggeler et al. [142]. Additional components are shown in red.

Damping resistances of 1.5, 3.3, 6.8 and 10 Ω respectively were added in series with the capacitances, to damp parasitic oscillations. These were sized to ensure that the resistor voltage was negligible (less than 5%) compared to the DC link voltage under maximum $\frac{dV}{dt}$ conditions, so that their effect on the switching process was insignificant.

This method could be particularly useful for controlling $\frac{dV}{dt}$ in integrated cascodes where it is not possible to access HV gate, such as in emerging co-packaged GaN cascodes.

Turn-on Figure 6.14a shows the effect of C_A on turn on $V_{D(casc)}$. Although there is a detectable reduction in $\frac{dV_{DS(casc)}}{dt}$ over the entire range of C_A , the effect is negligible. Additionally, for C_A at its maximum value of 100 pF, there is evidence of the onset of undesirable changes in switching behaviour, whereby the rate of fall of $V_{DS(casc)}$ tails off at lower voltages, with no meaningful reduction in the peak value of $\frac{dV_{DS(casc)}}{dt}$. This suggests that larger values of C_A may increase turn-on losses without any great improvement in control of the $V_{DS(casc)}$ transient.

The effect of C_A at turn-on could be increased by using a larger gate resistor. However, this can cause undesirable side effects. As shown in section 6.4, larger values of $R_{GH(LV)}$ lead to slower current rise-times and are therefore likely to unduly increase switching losses. Furthermore, it will be shown that the gate resistance chosen leads to a very significant reduction in $\frac{dV_{DS(casc)}}{dt}$ at turn-off. Although it is reasonable to use this method for different values of $R_{GH(LV)}$ and $R_{GL(LV)}$, the results reported by Aggeler et al. used a single gate resistor. Identical

values of $R_{GH(LV)}$ and $R_{GL(LV)}$ ensure these experimental results were obtained in a manner consistent with this previous work.

C_A caused no significant change to the $I_{D(casc)}$ waveform and it is therefore omitted from figure 6.14a for clarity.

Turn-off The effect of C_A at turn-off is substantial, despite the comparatively small size of $R_{GL(LV)}$. Small values of C_A of significantly less than the 50 - 80 pF of $C_{DG(HV)}$ have little effect on switching. However, the addition of 66 pF and 100 pF capacitances caused a very substantial reduction in $\frac{dV_{DS(casc)}}{dt}$, as can be seen in figure 6.14b.

The addition of C_A creates a new feedback path within a cascode device, during the already complex turn-off process. In this case, there is evidence that larger values of C_A can lead to this feedback tending towards instability, with substantial oscillations visible in both the $I_{D(casc)}$ and $V_{DS(casc)}$ waveforms. This feedback could be better damped by use of a LV transistor with a lower gain, to avoid the onset of the voltage rise period causing excessive voltage swings at the LV drain.

Some caution must be applied to the claim that the presence of large values of C_A limit $\frac{dV_{DS(casc)}}{dt}$. The overall voltage rise time is longer, but if it is oscillatory in nature as in figure 6.14b, peak $\frac{dV_{DS(casc)}}{dt}$ is not reduced substantially. Improved damping would improve the effectiveness of this method, by limiting peak $\frac{dV_{DS(casc)}}{dt}$.

The larger values of C_A that are required to limit $\frac{dV_{DS(casc)}}{dt}$ also limit the fall time of $I_{D(casc)}$. This happens because the presence of C_A fundamentally changes the turn-off process, altering the voltage imposed across the stray inductance that limit current fall. Whilst this will increase turn-off losses, the increase in current fall time due to C_A is smaller than corresponding increase in $V_{DS(casc)}$ rise time. This may make this method of $\frac{dV_{DS(casc)}}{dt}$ control more attractive than increasing the value of $R_{GL(LV)}$ when substantial reductions in turn-off $\frac{dV_{DS(casc)}}{dt}$ are required.

6.6.1.2 Method B: additional capacitance between HV drain and HV gate (C_B)

The effect of adding 33, 66 and 100 pF additional capacitance (C_B) between the SiC MOSFET drain and gate is shown in figure 6.15. Damping resistances of 4.7 and 6.8 Ω were added in series with the 66 and 100 pF capacitances respectively to damp parasitic oscillations.

The current waveforms were not significantly different from those recorded in figure 6.3 and did not change noticeably with increasing capacitance. They are therefore omitted from figure 6.15 for clarity. $V_{DS(LV)}$ showed a clear dependence on the additional capacitance at turn-off and is therefore plotted in figure 6.15b.

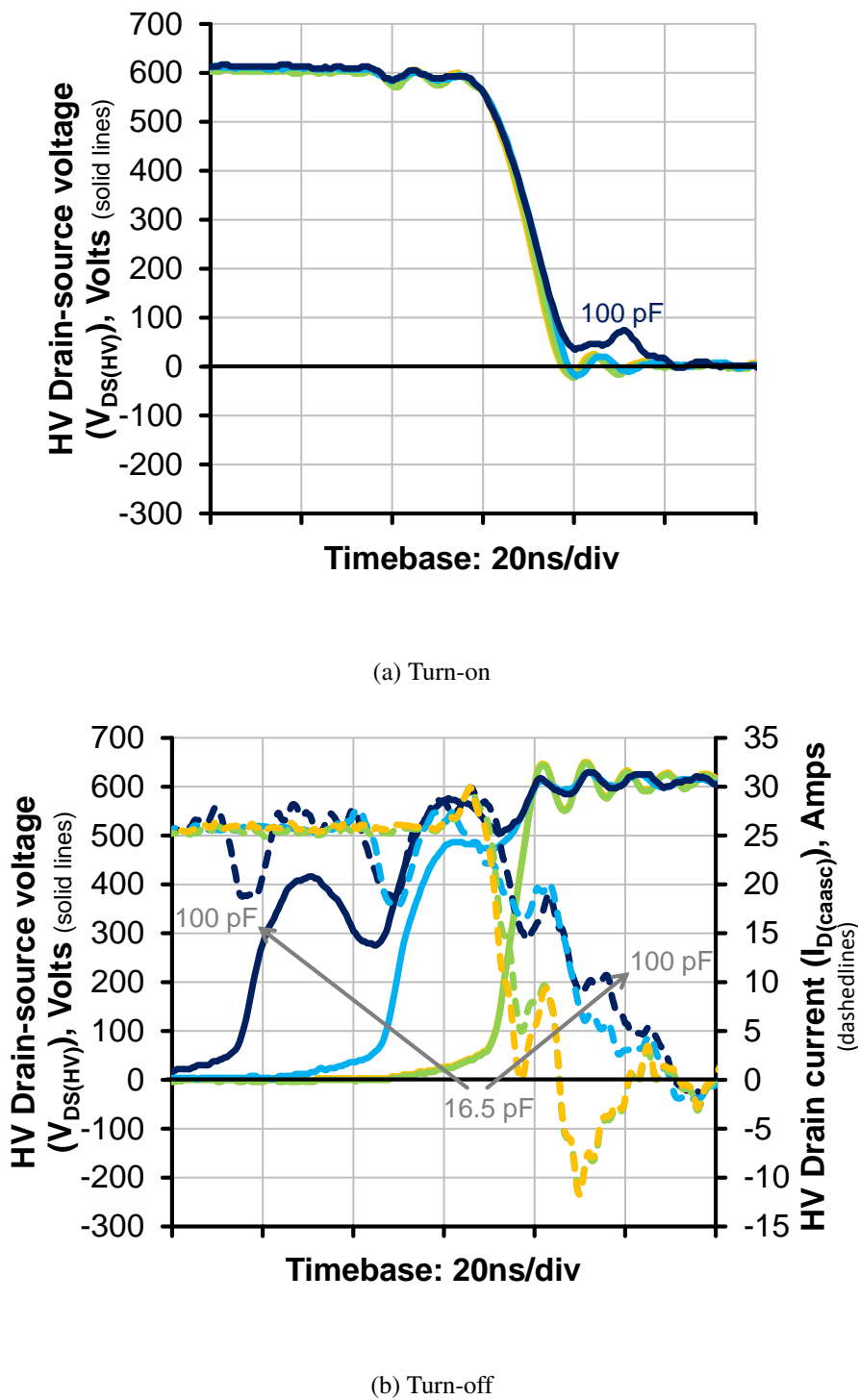
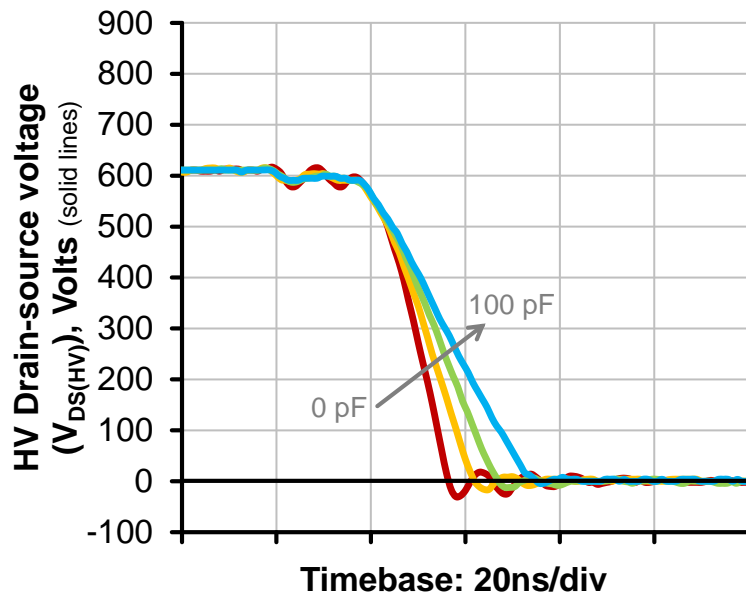
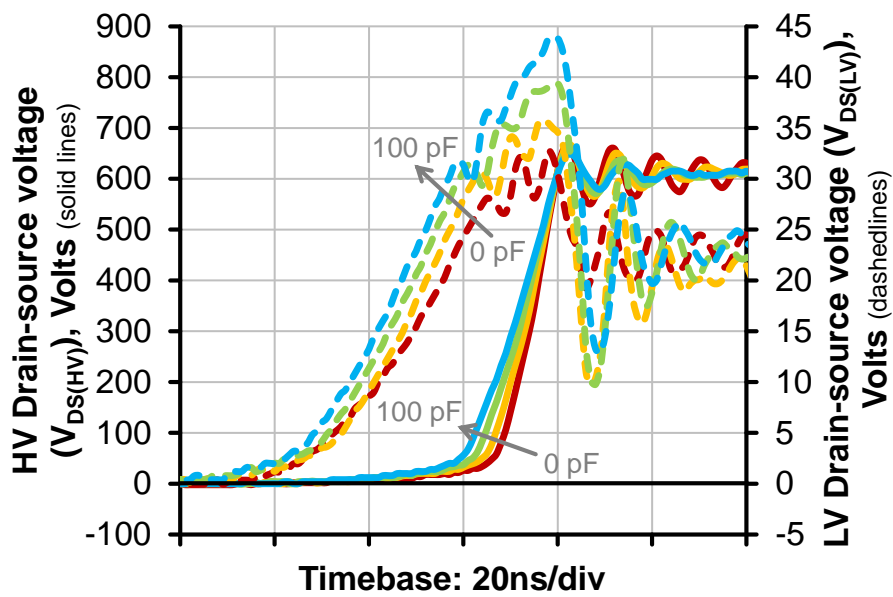


Figure 6.14: Effect of adding 0, 16.5, 33, 66 and 100 pF between SiC MOSFET drain and gate in cascode configuration.



(a) Turn-on



(b) Turn-off

Figure 6.15: Effect of adding 0, 33, 66 and 100 pF between SiC MOSFET drain and gate in cascode configuration.

Both turn-on and turn-off $\left| \frac{dV_{DS(casc)}}{dt} \right|$ are reduced approximately linearly by increasing C_B , due to the increased time constant of the HV gate circuit ($R_{G(HV)} \cdot (C_{DG(HV)} \parallel C_B)$). However, because of the differences between the turn-on and turn-off mechanisms in the cascode, switching speeds are not symmetrical and are not affected equally by C_B . In particular, the turn-off process, in which HV Miller current increases whilst $V_{DS(HV)}$ rises, ensures that $\left| \frac{dV}{dt} \right|_{off}$ is generally higher than $\left| \frac{dV}{dt} \right|_{on}$.

The slower rise of $V_{DS(HV)}$ due to increasing C_B allows $V_{DS(LV)}$ to rise further over the switching period and increases Miller current through $R_{G(HV)}$. This effect partially counteracts the effect of the increased capacitance, making C_B slightly less effective at reducing $\left| \frac{dV}{dt} \right|_{off}$ than C_A . This is apparent from the slightly slower reduction in $\left| \frac{dV}{dt} \right|_{off}$ compared to $\left| \frac{dV}{dt} \right|_{on}$ as C_B rises.

An important limitation of this method of $\frac{dV}{dt}$ control is the rated voltage of the LV switch. Figure 6.15b shows that $\hat{V}_{DS(LV)}$ increases approximately linearly with C_B at a rate of around 1 V for every additional 10 pF of capacitance. This is because the LV gate voltage continues to rise at a constant rate throughout the period in which $V_{DS(casc)}$ rises. Hence decreasing $\left| \frac{dV}{dt} \right|_{off}$ in this manner increases the time for which $V_{DS(LV)}$ rises whilst the HV transistor is switching and hence increases its maximum value.

Control of $\frac{dV}{dt}$ using this method must therefore be considered alongside the ratings of the LV switch. This point is not particularly apparent in the work of Aggeler, since the rise times of $V_{DS(casc)}$ investigated there were over five times longer than in these experiments.

This method of $\frac{dV}{dt}$ control gives reasonable control over both turn-on and turn-off voltage transients, without affecting current switching times. Its effect is similar to increasing the value of $R_{G(HV)}$, but has several advantages over that approach: The increase in $V_{DS(LV)}$ is smaller for a given amount of $\frac{dV_{DS(casc)}}{dt}$ control, since C_B does not also cause delay in the HV gate circuit, whilst the effect on $\frac{dV_{DS(casc)}}{dt}$ is more linear at both turn-on and turn-off since typically $C_B \ll C_{iss(HV)}$.

A drawback of this approach is that it requires access to the HV gate terminal. This method is therefore unsuitable for use with commercial co-packaged three-pin GaN cascodes

6.6.1.3 Choice of $\frac{dV_{DS(casc)}}{dt}$ control method

The addition of capacitance between the HV drain and LV gate in method A leads to a fundamentally different mode of operation compared to the basic cascode circuit. This approach may be helpful under specific circumstances and makes it possible to heavily limit turn-off $\frac{dV_{DS(casc)}}{dt}$ without affecting turn-on and with only a relatively modest effect on $I_{D(casc)}$. This could make it a useful way of making turn-on and turn-off $\frac{dV_{DS(casc)}}{dt}$ more equal, given the

propensity of the cascode to rapid turn-off. It is also the only method of controlling $\frac{dV_{DS(casc)}}{dt}$ at turn-off without using a very large value of $R_{GL(LV)}$.

However, method A raises concerns about stability and gate isolation. It is clearly very sensitive to even small changes in C_A and the potential for oscillation in the feedback mechanism it creates undermines its ability to limit $\frac{dV_{DS(casc)}}{dt}$. Furthermore, it eliminates the relative isolation of the LV gate from the switching process by directly coupling $V_{DS(casc)}$ transients into the LV gate. This has serious implications for the gate driver circuit, which is likely to require much more robust isolation to avoid these switching transients being coupled into the control system. Whilst method A has some advantages, the reliability and EMI issues that accompany it, significantly reduce its attractiveness.

Method B affects only the switching performance of the upper switch and does not fundamentally alter the overall behaviour of the cascode. It also limits the rise and fall of $V_{DS(casc)}$ in a very linear way. However, due to the positive feedback effects discussed in section 4.9.2, turn-on $\frac{dV}{dt}$ is reduced to a much greater extent than turn-off $\frac{dV}{dt}$. This is unfortunate, since $\frac{dV_{DS(casc)}}{dt}$ at turn-off is usually much larger than at turn on, which leads to a disproportionate increase in losses if this method is used to limit overall $\frac{dV_{DS(casc)}}{dt}$.

A drawback of both techniques is that increasing the capacitance between the LV or HV gates and the cascode drain increases the susceptibility of the gates to $\frac{dV_{DS(casc)}}{dt}$ transients across the switch. Particular care must therefore be taken when operating such a cascode switch in a bridge converter, where significant voltage transients may be imposed across the switches by the opposing transistor in a bridge leg. Appropriate selection of series damping resistance is also a requirement to avoid the addition of capacitance adversely affecting stability.

To control $\frac{dV_{DS(casc)}}{dt}$ in a practical circuit, a hybrid approach is likely to be advantageous. An effective strategy may be to choose a reasonably large value of $R_{GL(LV)}$ to limit both turn-on and turn-off $\frac{dV_{DS(casc)}}{dt}$ to approximately the same rate, before including additional capacitance using method B to further reduce overall $\frac{dV_{DS(casc)}}{dt}$ to the required value.

6.7 Cascode immunity to $\frac{dV}{dt}$ transients

In applications such as bridge circuits, where a pair of switches rapidly switch the voltage of a common node between a low and a high level, each switch can experience very high $\frac{dV}{dt}$ transients imposed by the other. Under these conditions, it is important that transients across a switch that has been turned off do not cause it to turn back on again. Furthermore, such transients must not be able to cause damage to either transistor, particularly to their sensitive gate circuits.

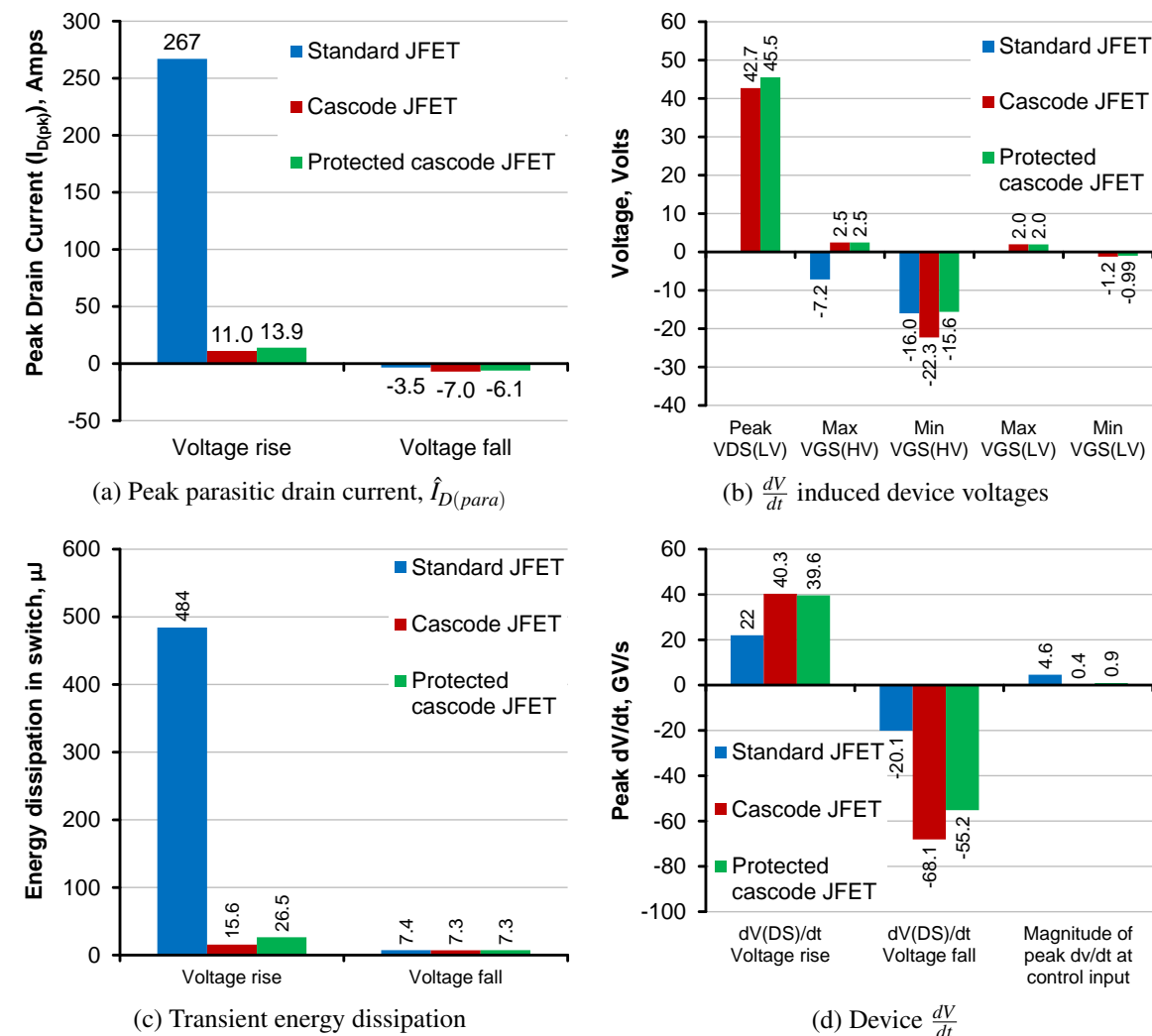


Figure 6.16: Comparison of simulated $\frac{dV}{dt}$ effects for individual JFET, cascoded JFET and TVS protected JFET cascode in single phase leg.

To investigate the effects of high $\frac{dV}{dt}$ on a cascode circuit in comparison with an individual transistor, an idealised phase leg circuit was simulated in SPICE. The phase leg was supplied from an ideal 600 V DC bus and was connected to an ideal 25 A constant current load sinking current to ground. The two power switches were modelled with ideal inverse parallel diodes to act as a freewheel path.

Three device combinations were compared. Both the SJDP120R085 SiC JFET and its cascode counterpart were simulated, using identical gate resistance to those described in section 6.3.2. Additionally, a 'protected' version of the same cascode circuit was tested. This featured an additional idealised 15 V bidirectional transient voltage suppressor (TVS) between the JFET gate and source, as well as a unidirectional 45 V TVS between the LV drain and source. These act to protect the HV and LV devices from excessive $V_{GS(HV)}$ and $V_{DS(LV)}$ respectively.

In each case, the upper device was switched from fully-off to fully-on and back, controlled by a 0 - 10 V pulse applied to its gate. The lower device was held with the gate driver input at -10 V for the individual JFET and at 0 V for the cascodes throughout the switching process of the upper device. This behaviour means that the drain-source voltage of the lower device is determined by the clamped inductive switching characteristic of the upper device.

To investigate the relative effectiveness of the individual device, cascode device and TVS-protected cascode in a bridge converter, the measured peak parasitic drain current, device voltage, transient energy losses and $\frac{dV}{dt}$ were compared. These comparisons are shown in figure 6.16

6.7.1 Peak drain current

A large $\frac{dV}{dt}$ imposed across a device can cause a large drain current by one of two mechanisms. Current will readily flow through the device's output capacitance, and can be of the order of several amps. This effect is unavoidable. The second mechanism is more problematic. A high positive $\frac{dV}{dt}$ flowing through C_{rss} in a transistor can cause enough current to flow through the gate resistors that the device's V_{GS} increases above V_T , causing the transistor to switch on. Although this condition persists only briefly, the transistor is unable to limit the current during this period and extremely high drain currents result.

This is clearly the case for the individual SiC JFET in figure 6.16a, for which a peak drain current of 267 A is measured during the period of positive $\frac{dV}{dt}$. This is nearly 20 times higher than either of the cascodes. This result may be explained by the differences in parasitics between the individual and cascode devices. For the individual JFET, the $\frac{dV}{dt}$ causes a rise in gate voltage sufficient for the device to briefly turn fully on.

In the cascode circuits, the behaviour is very different. The comparatively large value of $C_{GS(HV)}$ relative to $C_{DG(HV)}$ means that the displacement current due to the $\frac{dV}{dt}$ is primarily shunted to the HV source. Whilst the HV gate voltage increases due to this process, the HV source voltage increases much more, due to the high impedance of the LV switch. Therefore, instead of the $\frac{dV}{dt}$ increasing $V_{GS(HV)}$ in the cascode circuit, the opposite happens, causing the HV switch to switch off harder. This process is more effective in the unprotected cascode, since a more negative $V_{GS(HV)}$ can be achieved. However, this risks causing reverse breakdown of the HV JFET gate-source diode. Whilst this may be acceptable in a JFET, a similar effect in a HV MOSFET would cause catastrophic failure.

With a falling $\frac{dV}{dt}$, only capacitive currents are significant and peak parasitic drain currents are low. The magnitude of the currents is higher in the cascodes due to the higher $\frac{dV}{dt}$ switching capability of these devices.

6.7.2 Device voltages

The device voltages developed during periods of high $\frac{dV}{dt}$ are summarised in figure 6.16b. Of particular relevance is the effect of this transient on $V_{GS(HV)}$. Due to the mechanism described in the previous section, for the individual JFET the maximum value of $V_{GS(HV)}$ occurs during positive $\frac{dV}{dt}$ and the minimum during negative $\frac{dV}{dt}$. For the cascode circuits the situation is reversed.

The case for adding a protective TVS to the cascode is shown by the smaller magnitude of minimum $V_{GS(HV)}$ (for positive $\frac{dV}{dt}$). In the standard cascode without the TVS, $V_{GS(HV)}$ is limited by the breakdown voltage of the JFET gate-source junction; a situation that may be undesirable with a JFET and destructive for a MOSFET. However, limiting the magnitude of $V_{GS(HV)}$ in this way increases the voltage stress experienced by the LV MOSFET, as can be seen in the increase in $V_{DS(LV)}$ for the TVS protected cascode. Without the second TVS across the LV MOSFET, the effect of adding a TVS between the HV gate and source could be sufficient to cause breakdown of the LV device during periods of large positive $\frac{dV}{dt}$.

A further advantage of the cascode in high $\frac{dV}{dt}$ circuits is evident from the range of gate voltages experienced at the control input for each device (i.e. the range of $V_{GS(HV)}$ for the individual devices and the range of $V_{GS(LV)}$ for the cascodes). The individual JFET experiences a terminal input V_{GS} range of 8.8 V between the imposition of the positive and negative $\frac{dV}{dt}$ transients. However, the high internal resistance of the JFET means that the range of V_{GS} experienced by the JFET internally is even higher than this. The range of input gate voltage experienced by either cascode is less than half of this. With appropriate selection of LV device, it is possible to choose a cascode threshold voltage that guarantees that spurious turn-on of the LV device cannot happen, even when the switch experiences extreme $\frac{dV}{dt}$.

6.7.3 Transient energy dissipation

The currents caused by $\frac{dV}{dt}$ imposed across a device cause large instantaneous powers to be dissipated in the device. The total energy dissipated in each device is summarised in figure 6.16c.

Energy dissipation is much higher in the individual JFET during large positive $\frac{dV}{dt}$, due to the spurious turn-on effect that occurs in this device. This shows the value of the cascode circuit's ability to control $\frac{dV}{dt}$ -induced turn-on. The TVS protected cascode does suffer from higher energy dissipation during large positive $\frac{dV}{dt}$ as a consequence of device voltages being limited, but losses are still 18 times smaller than for the JFET alone.

There is negligible difference between the energy dissipation of the devices during large negative $\frac{dV}{dt}$.

6.7.4 Imposed dv/dt

The actual $\frac{dV}{dt}$ imposed across each device, as well as the magnitude of the maximum $\frac{dV}{dt}$ experienced at its control input is shown in figure 6.16. Due to the faster switching that is possible using a cascode circuit, both cascode devices experienced peak $\frac{dV}{dt}$ nearly twice as great as the JFET alone for a rising V_{DS} and approximately three times as great as the JFET alone for a falling V_{DS} .

This shows that cascode circuits are considerably better at both imposing and coping with very high $\frac{dV}{dt}$ events, particularly since the comparisons drawn between individual and cascode $\frac{dV}{dt}$ performance did not consider the difference in $\frac{dV}{dt}$ experienced by each device. This finding is supported by the magnitude of peak $\frac{dV}{dt}$ at the device control input, which is between 5 and 10 times higher for the individual JFET than for the cascodes. This implies that using a cascode device can also help eliminate the gate $\frac{dV}{dt}$ isolation problems associated with WBG devices.

The slight reduction in peak $\frac{dV}{dt}$ experienced by the TVS protected cascode shows that there is a small loss of performance associated with the addition of the TVS protection. However, this must be considered against the likely benefits of ensuring both devices always operate within their ratings.

6.7.5 Summary

The simulations presented here suggest that cascode circuits have advantages over individual transistors in circuits where high $\frac{dV}{dt}$ is anticipated. In particular, they naturally counteract

spurious device turn-on and provide good isolation of the control input from $\frac{dV}{dt}$ transients, leading to reduced power losses and less onerous gate isolation requirements.

A conventional cascode risks exceeding device ratings during high $\frac{dV}{dt}$ events, but this can be counteracted by the addition of TVS devices between the HV gate and source, and the LV drain and source. The addition of such protective components slightly reduces cascode performance, but ensures both devices operate within their specification under all operating conditions. Such components should be selected carefully to avoid adding excessive capacitance to the cascode, which could hinder switching performance.

6.8 Reverse recovery behaviour

6.8.1 Concerns

Concerns about cascode reverse recovery were raised by Domes and Zhang [135] who reported excessive losses when the cascode reverse conduction mechanism was used in a bridge converter. These losses were particularly concerning due to their magnitude: turn-on losses were reported to increase by 175 %, with a drain current overshoot of 250 %.

Such figures are a clear cause for concern and Domes and Zhang used them to justify the need for their 'Cascode Light' concept. However, their results are contradicted by others, who report excellent reverse recovery behaviour of GaN HEMT cascodes in similar topologies [121, 122].

6.8.2 Mechanism

The reason for such severe reverse recovery losses was described by Domes in terms of the change in effective C_{oss} of the cascode circuit during switching. When one switch transitions from conducting reverse current to blocking, $C_{oss(LV)}$ and $C_{GS(HV)}$ are initially connected in parallel with the cascode switch whilst the HV transistor channel still conducts. This means that the effective input capacitance of the cascode switch can be estimated as:

$$C_{oss(casc,initial)} = C_{oss(HV)} + C_{oss(LV)} + C_{GS(HV)} \quad (6.2)$$

until the HV channel is pinched off, before subsequently dropping to:

$$C_{oss(casc,final)} = C_{oss(HV)} \quad (6.3)$$

once the HV channel is pinched-off.

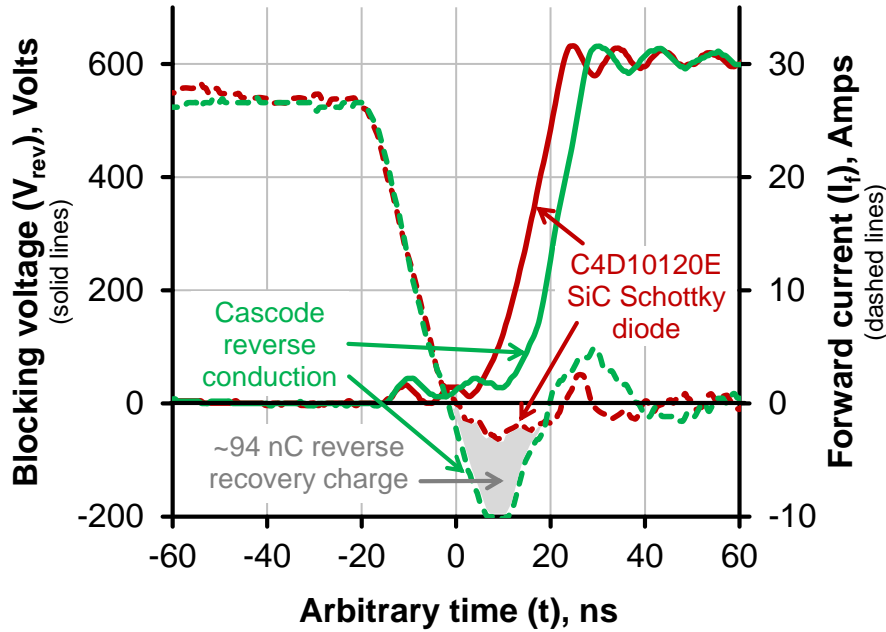


Figure 6.17: Comparison between reverse recovery of SiC MOSFET cascode (green) and SiC Schottky diode (red) when switching 25 A at 600 V. The grey area between the two current waveforms represents approximately 94 nC.

The large initial value of $C_{oss(casc)}$ and its sudden fall as blocking voltage increases was claimed to be the cause of the significant capacitive reverse recovery current. This effect is greater than would be expected for either the HV or LV devices alone, due to the combined effects of their capacitance.

6.8.3 Experiment

To investigate the discrepancies between authors, the reverse recovery of the SiC MOSFET/silicon MOSFET cascode described previously was compared with that of a C4D10120 SiC Schottky diode. This was done by substituting the free-wheel diode in the clamped inductive load set-up of figure 3.5 for the device of interest. The LV gate voltage of the cascode was held at 0V so that its reverse conduction was entirely passive.

The voltage across each device was switched, as for a standard clamped-inductive load test, using a SiC MOSFET/silicon MOSFET cascode to ensure rapid commutation of voltage and current to accentuate reverse recovery behaviour. The voltage and current experienced by the two devices is shown in figure 6.17.

6.8.4 Summary

There was a noticeably larger reverse recovery effect when cascode reverse conduction was used instead of a SiC Schottky diode. The additional reverse recovery charge was approximately 94 nC, which contributed to a reverse recovery current overshoot of 10.4 A, compared to 3.2 A for the Schottky diode. The resulting increase in turn-on loss in the lower switch during this period was estimated to be 258 μJ . This represents an increase in turn-on losses of 86% and an increase in overall switching losses of 60% compared to the measurements of figure 6.5.

Since reverse conduction through the cascode circuit is unavoidable even if an alternative rectifier is provided, a SiC MOSFET cascode converter with a free-wheel path through the power devices will experience switching losses that are 25% higher, than those of a converter that uses individual SiC MOSFETs and SiC Schottky diodes under the conditions investigated here. However, as shown in section 5.4, the reverse current used here is sufficiently large to ensure that some of it flows through the SiC MOSFET body diode. At least some of the additional reverse recovery current losses measured here must therefore be attributed to this, rather than the capacitive effects described by Domes.

Based on these measurements, using the cascode reverse conduction mechanism can lead to somewhat higher switching losses compared to when a SiC Schottky diode is used. However, as is clear from the literature [121, 122], this behaviour is strongly device dependent and the use of a HV device with a lower C_{GS} and a LV device with lower C_{oss} can significantly reduce the effect.

These findings support Domes' proposed mechanism to explain cascode reverse recovery. However, they strongly challenge his description of the severity of the effect. The extreme current overshoot and subsequent severe and very lightly-damped ($\xi < 0.05$) [196] ringing described in [135] are uncharacteristic of capacitive reverse recovery and are not apparent in figure 6.17 or in other published work.

From the description of the experimental work conducted by Domes, it appears likely that this behaviour is actually predominantly caused by substantial stray inductance in the switches being tested. This is particularly likely, since the power devices used by Domes were packaged in large (48×57 mm) packages intended for IGBT modules [197], which use through-hole pins to connect to the test PCB. These connections are an obvious source of additional stray inductance. An increase in the stray inductance increases the Q factor of the resonant circuit formed with the parasitic device capacitance, leading to the severe and under-damped oscillations observed.

Device capacitance can clearly have a detrimental effect on cascode reverse recovery behaviour. This can make overall cascode switching performance worse than for conventionally-

driven devices in some circumstances. These effects must be accounted for when choosing devices and may make cascode circuits less attractive in some topologies. However, cascode reverse recovery behaviour is not so severe as to make the circuit unusable in bridge configurations, and the justification for the 'cascode light' approach appears flawed, based on the experimental data presented here.

6.9 Conclusion

6.9.1 Device selection

The comparative performance of three state-of-the-art HV transistors has been investigated both when operating conventionally and when operated in a cascode circuit. By operating devices in a cascode configuration, overall switching losses can be reduced by 20 to 35 %, dependent on the exact devices used.

Of the devices investigated, the SiC MOSFET and SiC JFET are well suited to cascode operation. In particular, the switching transients are controllable with small to moderate values of gate resistance and are well within device ratings. A particular advantage of cascode operation for both SiC devices is the relative simplicity of their gate control, which circumvents the undesirable gate drive properties of both SiC devices.

Si SJ MOSFETs present several difficulties for cascode operation. Two trade-offs inherent to the super-junction design are particularly problematic: The large C_{iss} is responsible for switching delays which makes limiting $V_{DS(LV)}$ challenging and requires excessively large values of $R_{GL(LV)}$ to counteract, whilst the highly non-linear C_{DG} significantly limits turn on $\frac{dV_{DS(case)}}{dt}$ as a result of $\frac{dC}{dt}$ displacement currents.

In addition, the cascoded Si SJ MOSFET is easily capable of exceeding its $\frac{dV}{dt}$ rating at turn-off, leading to reliability concerns. It is not possible to control these turn-off transients without severely limiting the operation of the cascode. With a voltage rating also limited to slightly over half that of the SiC devices, there are no obvious advantages of using a Si SJ MOSFET in a cascode configuration in preference to either SiC device, apart from perhaps cost.

Despite the excellent high frequency performance of the LV GaN FET used in this experimental work, these properties are not useful in the cascode configuration, where switching performance is limited by the HV transistor. Instead, the robustness and low cost of the silicon MOSFET make it much more effective as a LV cascode transistor.

6.9.2 Gate resistance and stray inductance

Proper selection of gate resistance is extremely important for optimising cascode switching performance. The findings from this work validated the simplified switching model presented in chapter 4, although the range of gate resistances considered was also large enough to illustrate the limitations of this model. This was due to several of the underlying assumptions becoming invalid when very large gate resistances are used.

Minimising $R_{G(HV)}$ and $R_{GH(LV)}$ is beneficial for minimising switching losses. However, these resistances are helpful for damping parasitic oscillations and should be non-zero for this reason.

The magnitude of $R_{GL(LV)}$ is critical for matching the switching speed of the HV transistor to the LV transistor and hence limiting $V_{DS(LV)}$ at turn-off. To maximise switching speed, it should be selected to ensure that $V_{DS(LV)}$ approaches but can never exceed its rated value during the turn-off process. $R_{GL(LV)}$ can be used to some extent to limit turn-off $\frac{dV}{dt}$ without adversely affecting turn-on and can help to match turn-on and turn-off switching speeds.

Although stray inductance plays an important role in cascode stability, only stray inductance between the HV and LV devices has a significant effect on the switching waveforms. Large values of $L_{S(HV)}$ have a detrimental effect on turn-on current rise and peak $V_{DS(LV)}$ at turn-off. The presence of inductance in this location does help improve turn-on stability, with minimal effect on switching losses. However, a similar effect can also be achieved by increasing $R_{GH(LV)}$. Since it has a negligible impact on the turn-off current waveform, tuning $\frac{dI}{dt}$ by selection of $L_{S(HV)}$ is an ineffective method of $\frac{dI}{dt}$ control.

6.9.3 $\frac{dV}{dt}$ considerations

The rapid switching of the cascode circuit is one of its main attractions. However, in some applications, $\frac{dV}{dt}$ must be limited to ensure EMI requirements are met. It may also be desirable to match turn-on and turn-off $\frac{dV}{dt}$. Whilst this can be achieved by increasing gate resistances, this tends to result in non-linear voltage waveforms with disproportionately high switching losses.

Much more linear $\frac{dV}{dt}$ limitation is possible through the addition of drain-gate capacitance to the HV device as first suggested by Aggeler et al. [142]. However, an alternative approach suggested by the same authors, in which additional capacitance is added between the HV drain and LV gate was shown to be ineffective and to compromise stability.

The resilience of cascode devices to $\frac{dV}{dt}$ events is also of interest, particularly if they are to be applied to bridge circuits. By comparing the simulated performance of a single SiC JFET

under high $\frac{dV}{dt}$ conditions with that of a cascode using the same device, the cascode was shown to have greatly superior immunity to the undesirable affects associated with these events.

Very high $\frac{dV}{dt}$ imposed across a cascode device may exceed device ratings, but the addition of two TVS devices between the HV gate and source, and the LV drain and source was shown to protect the cascode from such conditions, at the expense of a modest reduction in $\frac{dV}{dt}$ immunity.

Cascode circuits can suffer from greater capacitive reverse recovery effects than standalone devices and this must be accounted for, particularly when using cascode switches in bridge converters. However, these effects can be managed by appropriate device selection.

Chapter 7

Conclusions

7.1 Summary

This work has shown that the WBG cascode circuit is not simply an academic curiosity, or an unwelcome compromise for driving awkward devices. Instead, cascode circuits offer distinct advantages when used to drive WBG transistors in fast switching circuits, which can improve reliability and reduce losses in power converters. The findings presented here form a clear and comprehensive guide to the benefits and practical application of the cascode circuit and remedy the lack of such information in the literature.

7.2 General conclusions

The most important benefit of cascode circuits is their ability to allow the input and output properties of the switch to be specified independently. Circuit designers are therefore free to use whichever HV device has the most appropriate switching and on-state characteristics for an application, without worrying about its drive characteristics. This eliminates concerns about the magnitude or variability of transistor threshold voltage and breaks the troublesome link between device ratings, stray capacitance and on-state resistance. Using a cascode circuit, it becomes feasible to design high voltage, high current unipolar devices with logic-level gate drive that do not risk spurious turn-on.

Cascode circuits are able to reduce switching losses in all types of high voltage FETs and benefit both enhancement-mode and depletion-mode devices. The SiC MOSFET in particular has been shown for the first time to benefit from operating in a cascode circuit. Other aspects of cascode dynamic behaviour are also advantageous in practical power converters: the convenient reverse conduction path through the cascode circuit can act as an effective alternative

to a discrete SiC Schottky diode if appropriate transistors are selected, whilst a well-designed circuit is able to withstand extreme $\frac{dV}{dt}$ stress without damage or unintentional turn-on.

The inevitably increased on-state resistance of cascode circuits remains a problem. However, this effect can be mitigated by appropriately biasing the HV transistor to partially compensate, as described in this work for the first time. Furthermore, the impact of the extra resistance of the LV transistor may often be overstated, especially in circuits that use HEMTs or JFETs. By allowing depletion-mode transistors to be used easily, cascode circuits avoid the need to use enhancement-mode variants of devices, which suffer from compromised on-state resistance and switching performance in comparison.

The idealised model of cascode switching developed here simplifies the understanding of the behaviour of circuit parameters during switching, whilst retaining a reasonable degree of accuracy. The value of this model is clear: A number of the inventions described in certain cascode patents can be seen to be logical developments by simply inspecting the variables of the model's equations [120, 125, 126].

Concerns about the lack of controllability of cascode circuits are largely unfounded and it has been shown analytically and experimentally that cascode switching can be effectively controlled by proper selection of gate resistors. Further studies have provided experimental evidence that supports and clarify other authors' work describing the optimum cascode layout [131] and methods of controlling voltage transients [142]. Additionally, after identifying flaws in previously published work [135], it has been shown that cascode circuits can be used effectively in bridge converters, despite a small reverse recovery penalty.

The main drawbacks of cascode circuits continue to be their increased on-state losses, circuit complexity and cost, as well as a widespread lack of familiarity with their operation. Whilst these disadvantages have previously been cited as reasons to avoid using cascode circuits, their specific advantages have often been overlooked. This work has clearly described the strengths and weaknesses of cascode circuits and shown that they are advantageous in appropriate applications when properly designed. The remaining part of this conclusion therefore distils the findings of this work into a simple set of design rules for any engineer considering using a cascode circuit in a power electronic converter.

7.3 Cascode design guide

7.3.1 Advantages of cascodes over standalone devices

Cascode circuits are best suited to high frequency applications, where low switching losses are more important than low on-state resistance. They are particularly helpful when using HV

transistors with excellent switching characteristics but undesirable gate drive characteristics such as: depletion-mode operation, low or variable threshold voltages, poor gain or transconductance, high voltage or bipolar drive requirements and semiconductor junction gates.

7.3.2 Suitable topologies

Switching losses in cascode circuits tend to be lower than for standalone transistors, particularly at turn-off. This makes cascodes an excellent choice for hard switched circuits and those with ZVS turn-on, including resonant and CrM topologies. Cascodes can be used effectively in bridge circuits, but care must be taken to avoid excessive capacitive reverse-recovery, which can cause increased losses.

7.3.3 HV device selection

For best switching performance, a HV transistor with a small C_{rss} and internal gate resistance is key. However, there is a trade off with on-state resistance, which tends to be inversely proportional to C_{rss} . A good compromise is achieved when switching and on-state losses are approximately equal under the intended operating conditions. Since losses in the LV transistor are small compared to those of the HV transistor, the cascode switch should be specified based on the properties of the HV transistor.

Voltage stresses on the LV device can be reduced by selecting a HV device with a low C_{iss} and C_{oss} . This will also help maximise turn-off switching speed. Turn-on losses are minimised in devices with a small internal gate resistance and C_{iss} and a maximum gate drive voltage that is much bigger than the threshold voltage.

Current rise times can be minimised by biasing the HV transistor gate at close to its rated voltage. However, some care is required to leave sufficient margin between the gate bias voltage and the rated gate voltage to avoid damage, particularly in MOSFET and HEMT devices. Devices with a reasonable margin between their threshold voltage and reverse gate breakdown voltage are also less likely to experience potentially damaging transients at turn-off.

The inductance at the source of the HV device directly limits current switching speed. HV devices in packages which minimise source inductance are therefore preferred, although this can lead to a trade-off with the need to heatsink them. Parasitic oscillations can be minimised further by using packages with low gate inductance. This can help minimise EMI, but has little effect on switching losses. Whether the HV device has a depletion-mode or enhancement-mode characteristic is largely irrelevant in a cascode configuration, although its threshold voltage does influence the rating of the LV transistor and choice of gate bias voltage.

7.3.4 LV device selection

To avoid excessive on-state losses, the LV transistor should have a small on-state resistance compared to that of the HV transistor, perhaps around 10%. However, care must be taken to select a device without excessive parasitic capacitance, which could increase switching losses. In most cases, it is beneficial to minimise C_{oss} to reduce turn-off HV gate-source voltage stress and to minimise reverse recovery current in applications where commutation is forced. However, when using cascode circuits in circuits with ZVS turn-on, the sum of $C_{oss(LV)}$ and $C_{GS(HV)}$ must be greater than $C_{oss(HV)}$, to avoid excess turn-on losses [124]. This additional capacitance may alternatively be supplied by an external capacitor in parallel with $C_{oss(LV)}$.

LV devices with smaller C_{iss} and C_{rss} are able to switch faster. However, unless these values are very large, the properties of the HV transistor will dictate switching speed and reducing LV on-state resistance should be targeted instead. Nevertheless, reducing C_{iss} does reduce the demands placed on the gate driver and devices with a small ratio of $\frac{C_{rss}}{C_{iss}}$ benefit from greater noise immunity.

The voltage rating of the LV transistor must be sufficient to avoid avalanche breakdown during switching. As a rule of thumb, the peak voltage it will experience during turn-off is approximately:

$$\hat{V}_{DS(LV)} = V_{bias} - V_{T(HV)} + \sqrt{\frac{2V_{DC}R_{G(HV)}C_{DG(HV)}(V_{T(LV)} - V_{GL(LV)})}{R_{GL(LV)}C_{DG(LV)}}$$

LV devices with higher voltage ratings can improve turn-off performance by forcing the HV transistor to switch faster, thus reducing turn-off losses. However, the benefits of a higher voltage device can easily be negated if it has a larger on-state resistance.

The threshold voltage of the LV transistor should be selected to suit the application. Higher values give greater noise immunity, although the LV gate is shielded from the most severe voltage transients by the HV transistor. Logic-level drive of a high voltage cascode is feasible, provided a device with reasonable transconductance and an adequately high threshold voltage is chosen.

The LV transistor is very sensitive to stray inductance at its source, so low inductance, surface mount packages such as PQFN are preferred. Package that permit a Kelvin connection to the transistor source are ideal. Heatsinking requirements for the LV device are not onerous and on-state losses are a small fraction of those of the HV transistor, typically $\frac{R_{DS(ON,LV)}}{R_{DS(ON,HV)}}$. Similarly, switching losses are very low compared to the HV transistor, since the LV device experiences resistive switching at turn-on and peak turn-off voltage is small compared to that of the HV transistor.

Care must be taken in applications which require reverse conduction through the cascode, to minimise losses due to reverse recovery of the LV transistor body diode. Devices with a low Q_{rr} rating are preferred here.

7.3.5 Layout considerations

Good layout is important to maximise switching performance and minimise radiated EMI. Minimising cascode source inductance is the key priority and this can be achieved using a low-inductance package for the LV device with a Kelvin connection for the gate drive ground reference. Next, the inductance between the HV source and LV drain should be minimised by placing the two devices as close together as physically possible. Cascode drain inductance is less of a concern, but minimising it will help to control EMI.

The sensitivity of the LV transistor to radiated fields can be reduced by minimising the loop area between the gate drive and ground reference tracks. This can be done by simply routing the two connections on top of each other, on adjacent layers of a PCB. Similarly, the connection between the HV gate and cascode source should have as small a loop area as possible to avoid sensitivity to and radiation of interference. For best results, the HV gate connection to the cascode source should also be through a Kelvin connection to avoid amplifying ‘ground bounce’ oscillations.

In cascodes that use a non-zero bias voltage on the HV gate, the connection to the cascode source is through a decoupling capacitor. This should be a low ESR ceramic type that is much larger than the HV device input capacitance and must be placed to minimise the size of the loop between the HV gate and cascode source. It must be capable of handling the entire HV Miller current. Layout of the connection to the biasing voltage source is not critical and may benefit from a resistor or choke to prevent conducted high frequency interference from reaching power supplies.

7.3.6 Choice of HV bias voltage

The HV transistor bias voltage determines its on-state resistance and influences turn-on losses, with larger values reducing both. However, higher bias voltages directly increases the voltage stress on the LV transistor, which must be adequately rated to deal with this. It is also important to leave an adequate margin between the bias voltage and the rated HV gate breakdown voltage to avoid damage from the gate from switching transients.

7.3.7 Gate drive

A high current gate drive is not usually required due to the large gain of the cascode circuit, so standard MOSFET gate driver ICs should be suitable. However, for optimum performance, a gate driver with connections for separate turn-on and turn-off resistors is mandatory.

In most cases, a small $R_{G(HV)}$ (of the order of $1\ \Omega$) is helpful for damping oscillations and does not significantly affect switching losses. Ringing in the HV gate circuit can be remedied by increasing $R_{G(HV)}$, but this directly increases switching losses and also requires much larger values of $R_{GL(LV)}$ to avoid excessive voltages across the LV transistor. If HV gate oscillations are a problem, layout improvements may be more effective.

Precise switching behaviour is strongly layout dependent. It is recommended that in any new design, gate resistor sizes are overestimated. They can be reduced at a later stage when device switching behaviour is measured experimentally. $R_{GL(LV)}$ should be expected to be much larger than $R_{GH(LV)}$ and these two gate resistors may normally be expected to be of the order of a few tens of ohms and a few ohms respectively.

When maximising switching speed, the optimum value of the turn-on resistor $R_{GH(HV)}$ is one that is large enough to damp voltage oscillations at the LV drain, but is small enough to avoid significantly limiting the rate of rise of drain current. It will typically also be the value that gives a critically-damped voltage rise at the LV gate. The optimum value of $R_{GL(LV)}$ is the smallest value which both limits $\hat{V}_{DS(LV)}$ and $\hat{V}_{GS(HV)}$ to below their respective breakdown voltages, whilst also allowing for an adequate safety margin.

Users of cascode circuits should be aware that the turn-off delay is typically much longer than the turn-on delay and this must be accounted for in the gate drive circuitry.

7.3.8 Circuit protection

The two most vulnerable parts of the cascode circuit are the drain of the LV transistor and between the gate and source of the HV transistor. Excess voltages here can cause avalanche breakdown which may reduce reliability. In the case of HV MOSFETs, the device may even be destroyed.

Breakdown at these locations should not occur during normal hard-switching conditions, providing $R_{GL(LV)}$ has been chosen correctly and $C_{oss(LV)}$ is not excessively large. However, when using HV transistors with large leakage currents, a TVS diode in parallel with the LV switch is recommended to avoid avalanche breakdown of the LV switch during long periods of voltage blocking.

In circuits such as bridge converters where high $\frac{dV}{dt}$ transients are expected to be imposed across the cascode, high speed TVS diodes should be fitted between the LV drain and source

and HV gate and source. This should be capable of limiting transient voltages to comfortably within the device ratings, even at currents of several amps. The HV gate-source TVS must be bi-directional. Surface mount, low capacitance TVS diodes are preferred and must be mounted as close to the transistors as possible to minimise parasitic inductance and EMI. Correctly chosen TVS diodes enable the cascode circuit to withstand extreme $\frac{dV}{dt}$ transients, without the risk of damage or spurious turn-on.

In circuits where gate driver isolation is a concern, the addition of capacitance in parallel with $C_{GS(LV)}$ will further reduce the sensitivity of the LV transistor gate to $\frac{dV}{dt}$ transients. This comes at the expense of increased switching delays. As with other HV transistors, cascode switches must be suitably isolated from control circuitry.

7.3.9 Reverse conduction

Reverse conduction through the cascode circuit can be used as an alternative to an inverse parallel Schottky diode to reduce cost and component count. Reverse conduction occurs automatically whenever the cascode is subject to a reverse voltage greater than the forward voltage of the LV transistor body diode. Reverse conduction losses are dominated by the channel resistance of the HV device. However, they can be reduced slightly by the addition of a silicon power Schottky diode in inverse parallel with the LV transistor, or by actively switching on the LV transistor during reverse conduction.

Care must be taken not to exceed the rated HV gate-source voltage during reverse conduction, since it experiences the voltage drops across both devices in addition to V_{bias} . Reverse conduction is therefore less advisable in HV devices with a small margin between V_{bias} and the breakdown voltage are used. If a HV SiC MOSFET is used, the voltage drop across its channel must be lower than the forward voltage of its body diode to avoid additional reverse recovery losses due to its body diode.

Cascode reverse conduction is associated with greater reverse recovery current than for standalone devices, which can lead to higher overall switching losses. These effects can be minimised by choosing a HV device with low C_{GS} and a LV device with a low C_{oss} . Cascode reverse recovery losses are mitigated by the fact that a discrete free-wheel diode is no longer required and switching losses associated with its parasitic capacitance are therefore eliminated from the circuit. The cascode reverse conduction mechanism only works when FETs or HEMTs are used as the HV device, since these are capable of bi-directional channel conduction.

7.3.10 Control of switching transients

The cascode is effective in circuits where fast switching is required. It may not be the best choice when $\frac{dV}{dt}$ and $\frac{dI}{dt}$ limits are necessary. There is no practical way of limiting the current transients without excessively affecting switching or on-state losses. An alternative switch should be sought if this is a concern.

To limit switching $\frac{dV}{dt}$ to a specified value, additional drain-gate capacitance should be added to the HV device to reduce turn-on $\frac{dV}{dt}$. This must be able to handle several amps of Miller current as well as the entire blocking voltage of the cascode. The use of a low inductance package and a series damping resistance will help to mitigate any parasitic oscillations. $R_{GL(LV)}$ should then be increased until peak turn-off $\frac{dV}{dt}$ is below the required limit.

7.4 Further work

The work presented in this thesis is of a fundamental nature, due to the need to explore the very detailed operation of the WBG cascode circuit. A useful direction for further work would therefore be to construct an ‘ideal’ cascode based on the guidelines presented here and to experimentally investigate its behaviour in a practical application. Some areas of particular interest for future work include:

- A comparative test between cascode and conventional devices in a high frequency bridge converter, taking advantage of cascode reverse conduction behaviour. Particularly valuable device performance comparisons would could be made between:
 - SiC MOSFET cascodes and conventionally-driven SiC MOSFETs.
 - A commercial co-packaged HEMT cascode and an optimised discrete GaN HEMT cascode, constructed using the design optimisations described here such as operation with a positive HEMT gate bias voltage.
 - An optimised SiC MOSFET cascode and an optimised GaN HEMT cascode.
 - The reverse conduction behaviour of an optimised cascode and a SiC Schottky rectifier
- Investigating the cascode as a high-current switch, using a number of paralleled HV devices controlled by a single LV transistor. Based on the results presented here, this appears to be feasible for devices with a positive on-state resistance temperature coefficient, such as JFETs. However, the dynamic behaviour of such a device would require careful analysis.

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- Using the design rules described in this work to develop an integrated cascode-based driver for WBG devices. This could include an optimised LV MOSFET, as well as isolation and circuit protection. By using feedback at the drain of the LV switch, the gate drive of the cascode could be optimised to maximise switching speed without risking parasitic oscillations.
 - Further investigation of topologies that are well suited to the fast turn-off ability of the WBG cascode circuit. This could include ZVS turn-on converters and pulsed power applications.
 - An investigation of the performance of SiC BJT cascode circuits

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Appendix A

Semisouth SiC JFET SPICE model

The following model statement is the SPICE model of the Semisouth SiC vertical JFET model described in chapter 4. It was provided by Kevin Speer of Semisouth on 26/09/2012.

```
.subckt SJDP120R085 D G S
.param R=530m ; R_gate
Bg G Gi I=-UpLim(47m*
+ uRamp(V(D,Di))*3.5,10,1)/R
Rg G Gi {R} tc=-3m
Rd D Di 70m tc=4m 40u
Csd S Di 3p
Cgd G Di 13p
Ji Di Gi S SJDP120R085
.model SJDP120R085 njf
+ Vto=-4 Beta=45 B=30m
+ Lambda=500u Vk=2k5 Alpha=20u
+ Is=1f N=3.4 + Isr=1n Nr=6.8
+ Cgd=1n Cgs=610p Pb=2.6 M=0.92
+ Kf=100f Af=1
+ VtoTC=-2m4 BetaTCe=-0.65 Xti=86
.ends SJDP120R085
```


Appendix B

SiC JFET hybrid model

A SPICE model sub-circuit for the hybrid SiC JFET model used in [chapter 4](#) is listed here:

```
.subckt SJDP120R085_hybrid D G S
M1 Di Gi Si Si Channel
M2 Di Gi Si Si Capmodel
DGS1 G Si DiodeGS
DGD1 G Di DiodeGD
Rd1 D Di 49m
Rs1 Si S 15m
Rg1 Gi G 5
.model Channel NMOS(LEVEL=3 VT0=-5.24 KP=18.6 VMAX=1E5
+ L=2.2E-6 Ld=9E-7 W=1.5E-6 Phi=0.15 Gamma=0 Delta=1.12
+ Nsub=1E16 Rd=0 Rs=0 U0=1000 Is=0 CBD=0 CBS=0 CGS0=0
+ XJ=0 TOX=0.5E-6 Pb=0 CJ=0 KAPPA=1 ETA=0 THETA=0.1 TPG=0)
.model Capmodel VDMOS(VT0=1.5k Kp=0 CJO=0 CGS=175p Cgdmax=2.5n
+ CgdMIN=25p IS=0 VJ=1.5k Rd=0 Rg=0 Rs=0 Rb=1G A=0.15)
.model DiodeGS D(Ron=0.28 Roff=1G Vfwd=2.4 Epsilon=2.15
+ Vrev=22 Rrev=0.28)
.model DiodeGD D(Ron=0.28 Roff=1G Vfwd=2.4 Epsilon=2.15)
.ends SJDP120R085_hybrid
```


Appendix C

PCB design drawings

C.1 Schematics

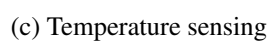
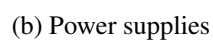
Schematic drawings of the test PCB are shown in figure C.1. Figure C.1d shows various sub-circuits referred to multiple times in figure C.1a. For brevity, only one instance of each is reproduced.

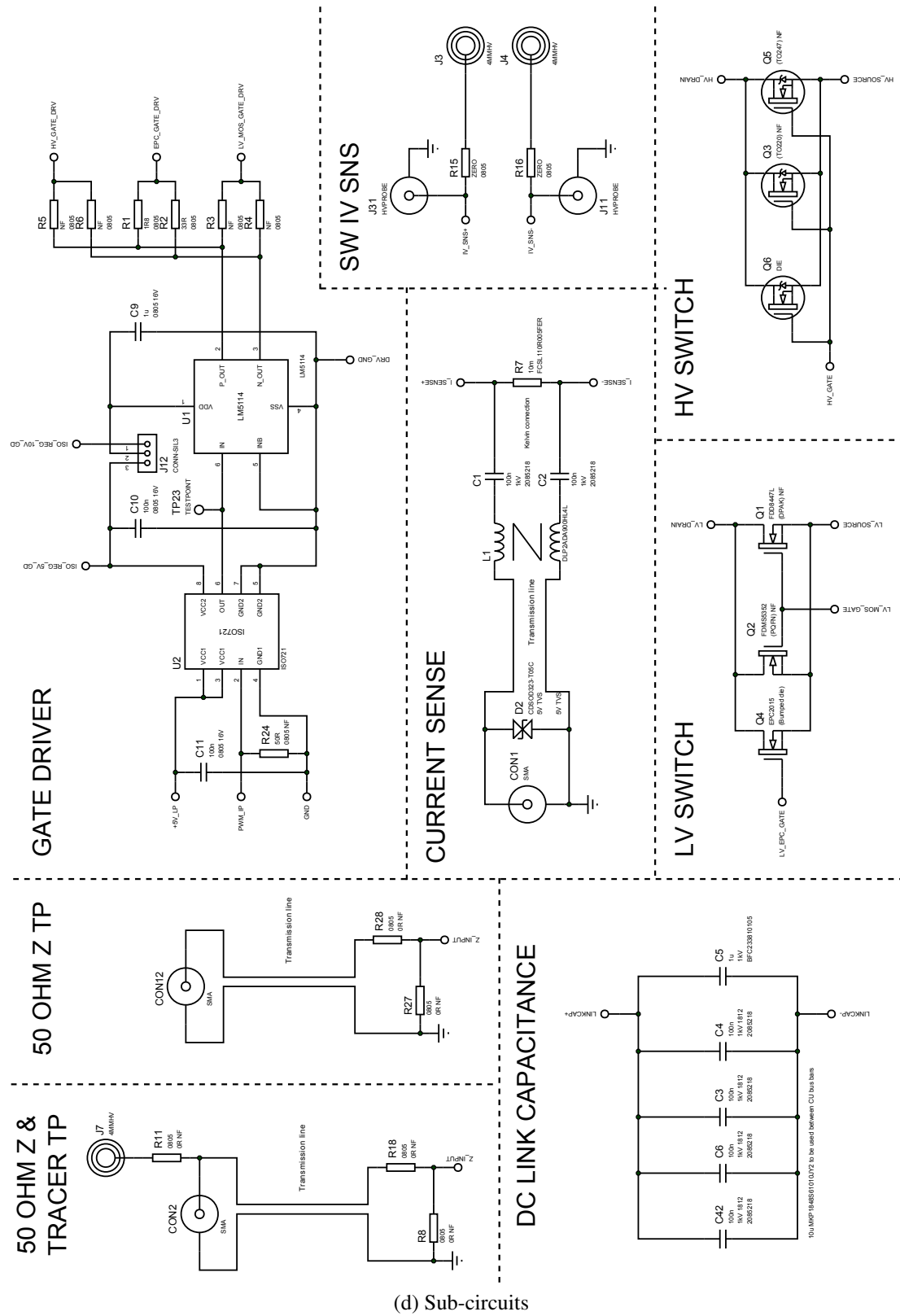
C.2 Layout

The PCB layout is shown in figure C.2. The actual size of the PCB is 75×160 mm. The layouts shown here have been reduced in size slightly for reasons of space.



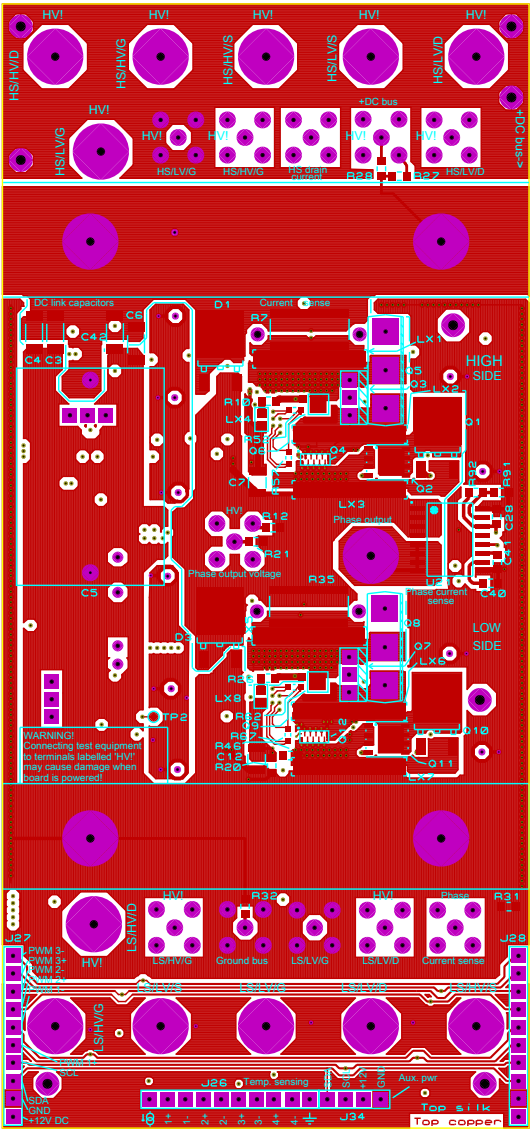
(a) Overview



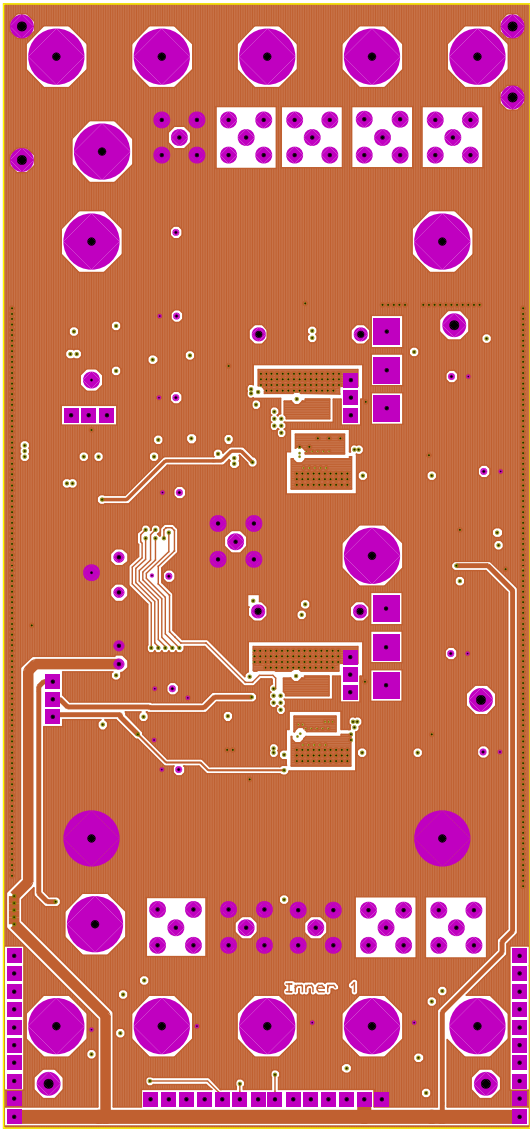


(d) Sub-circuits

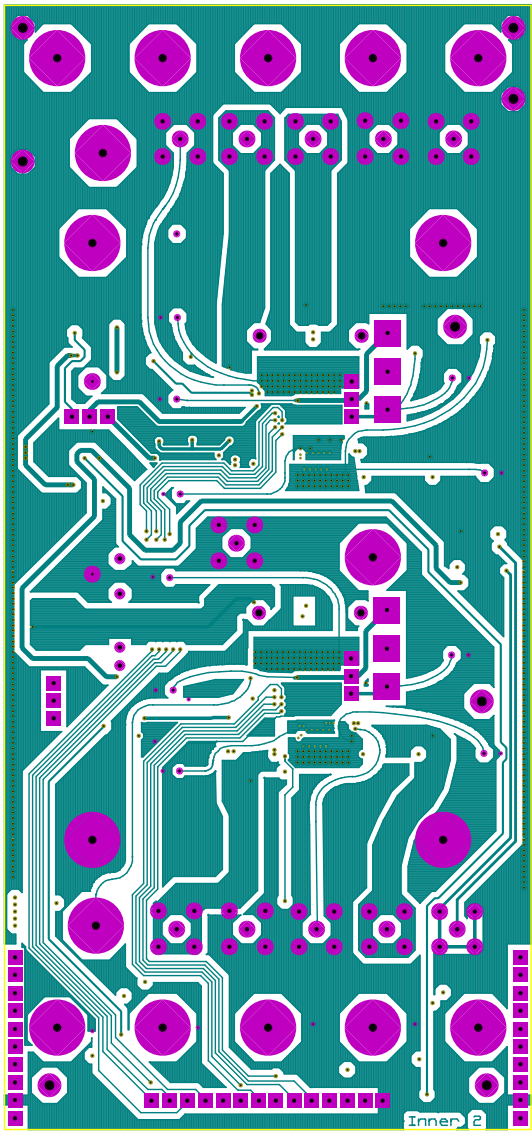
Figure C.1: Test PCB schematic drawings



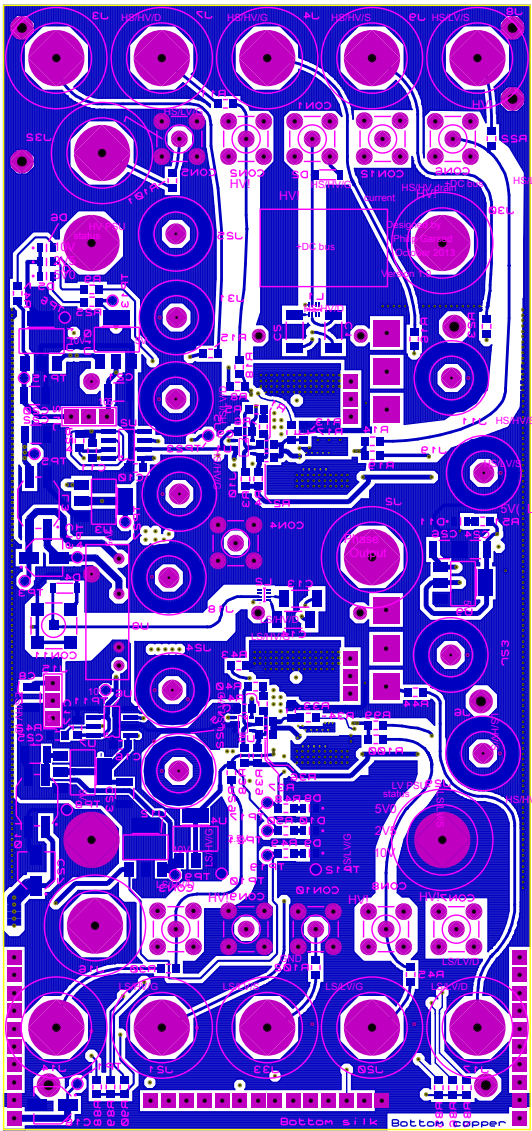
(a) Top copper (layer 1)



(b) Ground plane (layer 2)



(c) Tracking (layer 3)



(d) Bottom copper (layer 4)

Figure C.2: Test PCB layout

Appendix D

Clamped inductive load driver code

The code below is that used to drive the clamped inductive load used in the experimental work. It is written for the Microchip C30 compiler:

```
#include <stdio.h>
#include <stdlib.h>
#include "p30f2020.h"
#include "config.h"

#define FCY 30000000UL //Set frequency (Fp11/16)
#include <libpic30.h>

int main(int argc, char** argv) {

    LATEbits.LATE5=0;                // Ensure output is off

    float inductance = 111.4;        //Set system inductance in uH
    float vdc = 600;                 //Set DC bus voltage in volts
    float ipeak = 25;                //Set desired peak current in amps
    float timeout = 0;               //Set desired reset timeout in seconds

    __delay_ms(timeout*1000);        //Allow Programmer time to settle down!

    //Calculate turn off delay in us based on inductance, voltage and desired current
    float turn_off_delay = inductance*ipeak/vdc;
    int delay_cycles = turn_off_delay * FCY / 1000000;

    ADPCFG=0xFFFF;                 //Set all pins to digital IO
    TRISB=0;                        //Set PORTB to output
    TRISE=0;                        //Set PORTE to output

    //Initial setup
    TRISBbits.TRISB1 = 1;           //Set pin B1 to input for trigger switch
    LATBbits.LATB0=0;               //Turn dev board LED off
    LATBbits.LATB1=0;               //Make sure no output on input latch!
    LATBbits.LATB2=1;               //Switch green LED on
    LATBbits.LATB3=0;               //Switch red LED off
    LATEbits.LATE5=0;               //Make sure output still off!
```

```

while(1)      //Main loop
{
    LATEbits.LATE5=0;      //Make sure output STILL off!
    LATBbits.LATB0=0;      //Turn dev board LED off

    //Wait for user input from switch
    while( PORTBbits.RB1 == 0 )
    {
    }

    //Turn light to red
    LATBbits.LATB3=1;      //Switch red LED on
    LATBbits.LATB2=0;      //Switch green LED off
    LATBbits.LATB0=1;      //Turn dev board LED on
    LATEbits.LATE5=1;      //Switch output on

    __delay32(delay_cycles); //Allow inductor current to rise to required value

    LATEbits.LATE5=0;      //Switch output off
    LATEbits.LATE5=0;      //for 200ns
    LATEbits.LATE5=0;      //We waste cycles here:
    LATEbits.LATE5=0;      //low level commands
    LATEbits.LATE5=0;      //are simply too slow!
    LATEbits.LATE5=0;

    LATEbits.LATE5=1;      //Switch output on
    LATEbits.LATE5=1;      //for second edge of interest
    LATEbits.LATE5=1;      //Again we waste cycles
    LATEbits.LATE5=1;
    LATEbits.LATE5=1;
    LATEbits.LATE5=1;

    LATEbits.LATE5=0;      //Turn output off

    __delay_ms(500);      //Delay to avoid overheating DUT

    LATBbits.LATB2=1;      //Switch green LED on

    while( PORTBbits.RB1 == 1 )    //Wait until switch is 'unpressed'
    {
        //LED Amber if switch still pressed
    }
    LATBbits.LATB3=0;      //Turn red LED off
}

return (EXIT_SUCCESS);
}

```

Appendix E

Effects of HV gate and drain inductance

Figures E.1 and E.2 show the effects on switching behaviour of additional inductance at the cascode HV drain and source respectively. They are referred to in section 6.5.

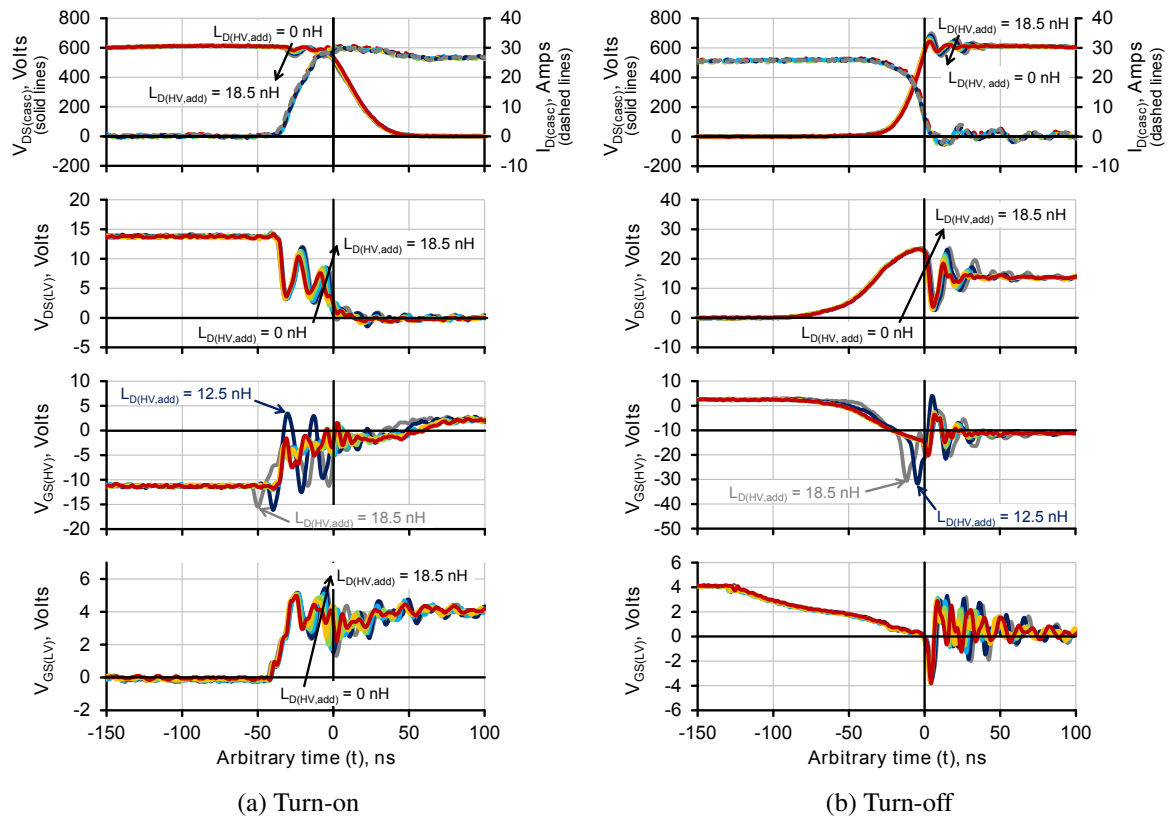


Figure E.1: Switching waveforms for $L_{D,add} = 0, 2.5, 5, 8, 12.5$ and 18.5 nH

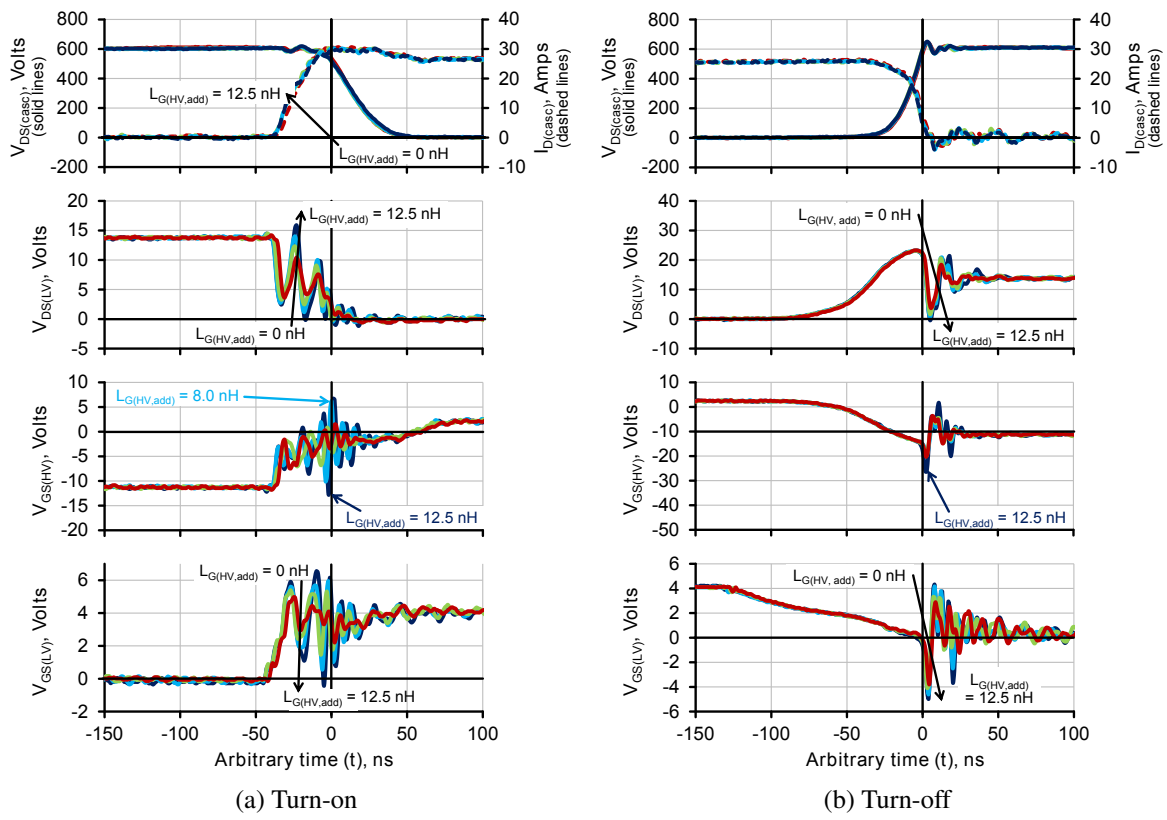


Figure E.2: Switching waveforms for $L_{(G,add)} = 0, 2.5, 5, 8$ and 12.5 nH